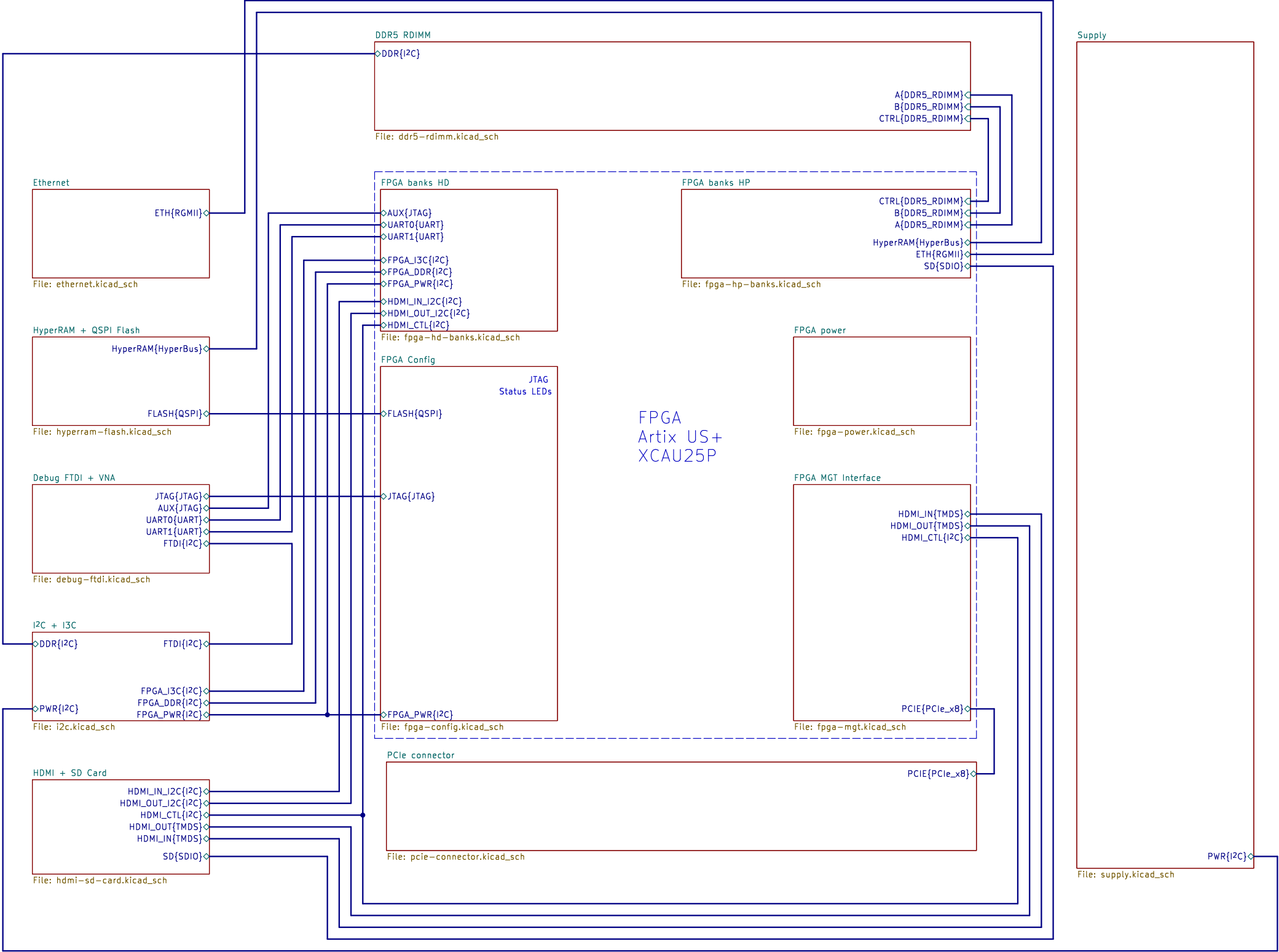


RDIMM DDR5 Tester



FPGA
Artix US+
XCAU25P

Mechanical

A1
Heatsink_ATS-61500R-C2-R0

Horizontal
lightguide
1x3
H2
Lightpipe_Mentor_1296.2013

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Antmicro
Sheet: /
File: data-center-rdim--ddr5-tester.kicad_sch

Title: RDIMM DDR5 Tester

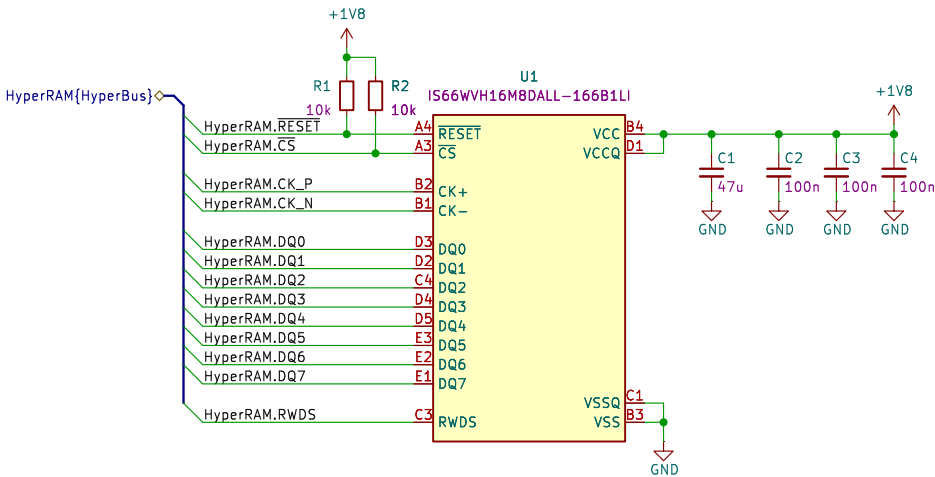
Size: A3
KiCad E.D.A. 9.0.6

Date: 2024-12-20

Rev: 2.1.0:2ebd8152
Id: 1/17

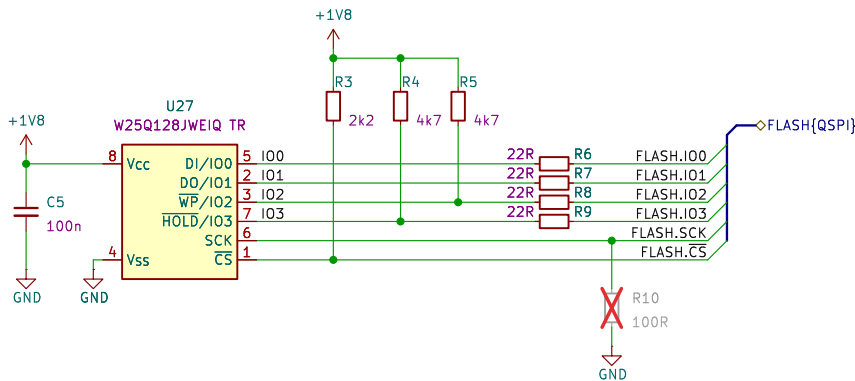


HyperRAM

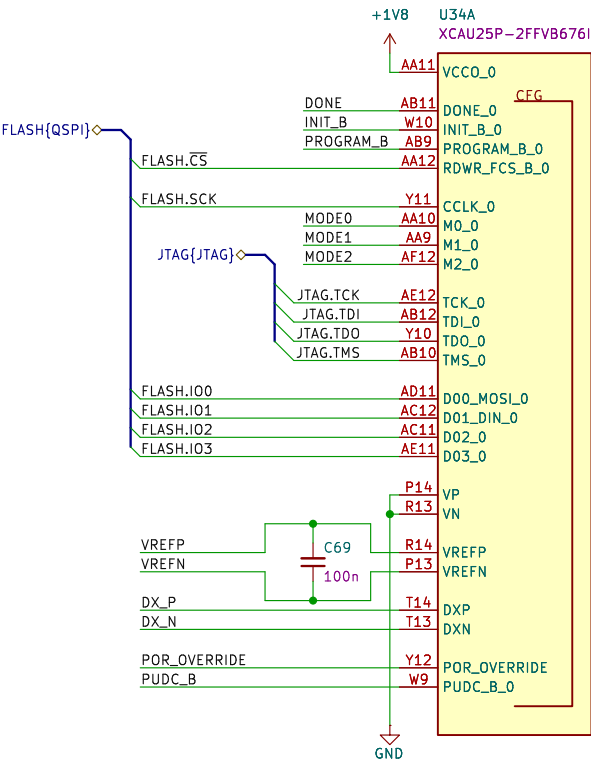


(Q)SPI flash

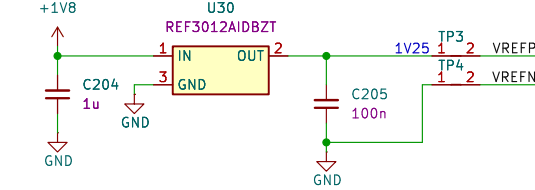
Master SPI Quad (x4) configuration scheme
Follows FPGAs Configuration User Guide UG570



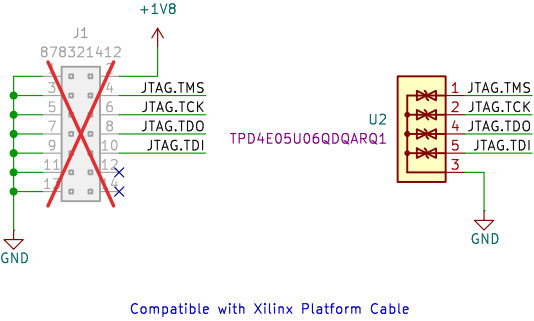
FPGA BANK 0



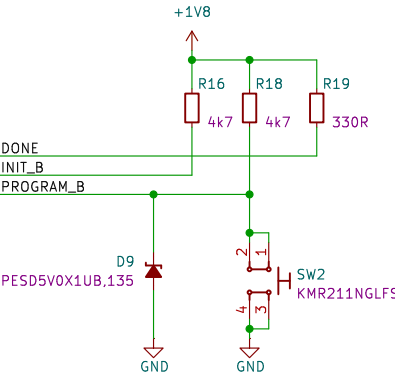
LDO



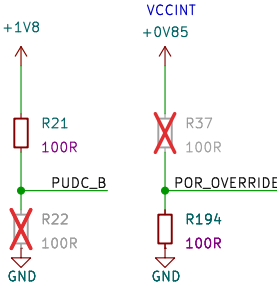
JTAG Connector



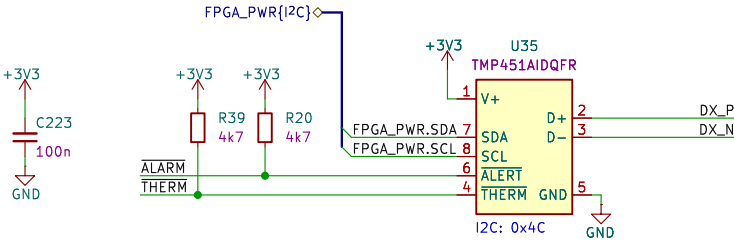
Pull-ups



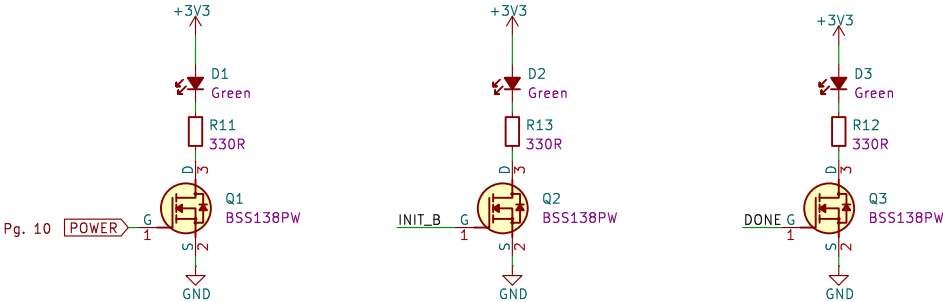
Probes



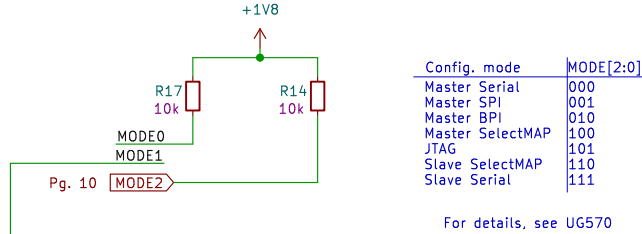
Temp sensor



STATUS LEDs



Configuration Modes



DDR5 RDIMM connector

Subchannel A

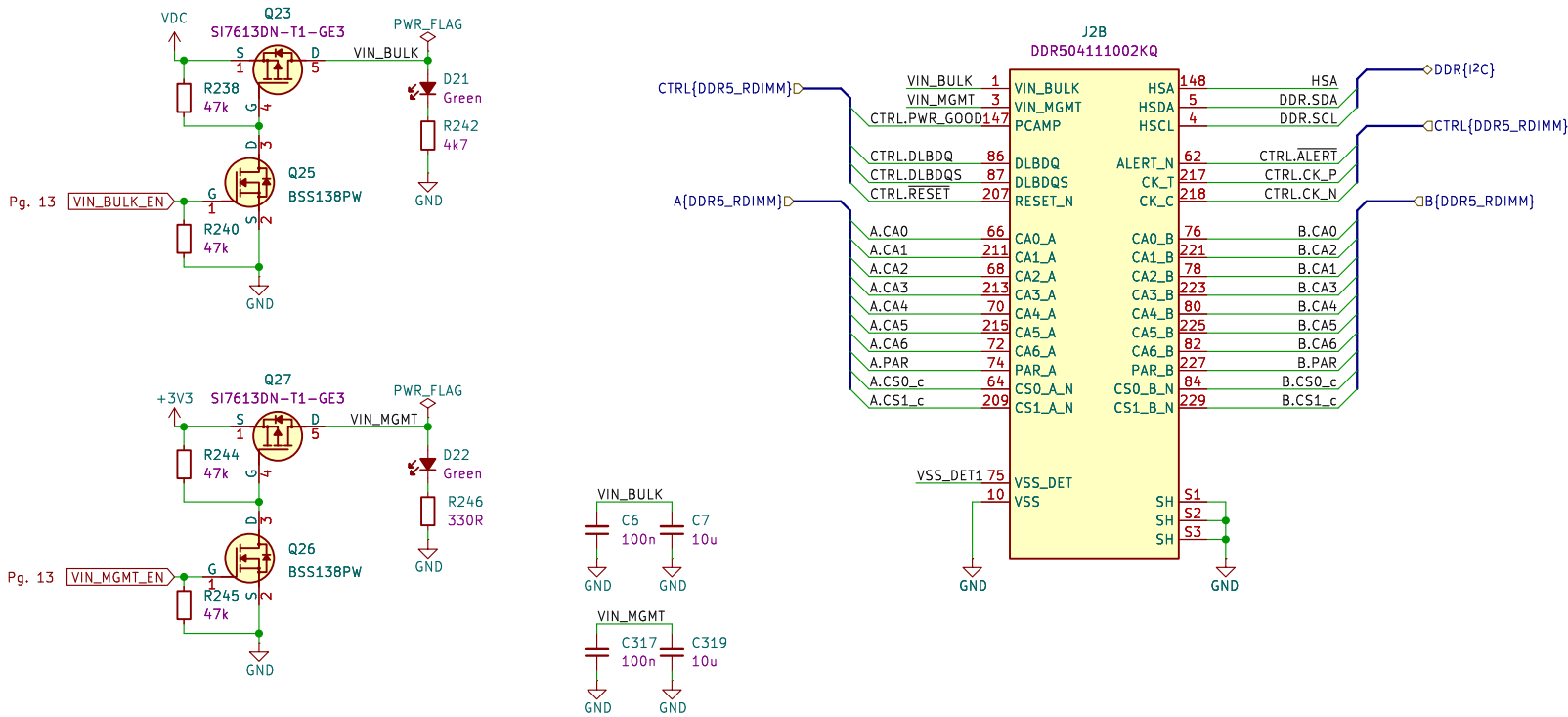
Subchannel B

A{DDR5_RDIMM}

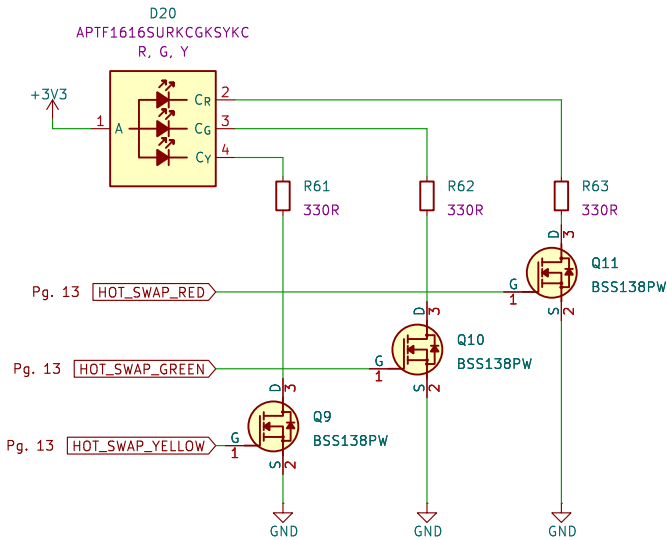
B{DDR5_RDIMM}

J2A DDR504111002KQ											
A.DQ0	7	DQ0_A	DQ0_B	100	B.DQ0						
A.DQ1	9	DQ1_A	DQ1_B	102	B.DQ1						
A.DQ2	153	DQ2_A	DQ2_B	245	B.DQ2						
A.DQ3	154	DQ3_A	DQ3_B	247	B.DQ3						
A.DQS0_P	11	DQS0_A_T	DQS0_B_T	104	B.DQS0_P						
A.DQS0_N	12	DQS0_A_C	DQS0_B_C	105	B.DQS0_N						
A.DQ4	14	DQ4_A	DQ4_B	107	B.DQ4						
A.DQ5	16	DQ5_A	DQ5_B	109	B.DQ5						
A.DQ6	159	DQ6_A	DQ6_B	252	B.DQ6						
A.DQ7	163	DQ7_A	DQ7_B	254	B.DQ7						
A.DQS5_P	157	DQS5_A_T	DQS5_B_T	250	B.DQS5_P						
A.DQS5_N	158	DQS5_A_C	DQS5_B_C	249	B.DQS5_N						
A.DQ8	18	DQ8_A	DQ8_B	111	B.DQ8						
A.DQ9	20	DQ9_A	DQ9_B	113	B.DQ9						
A.DQ10	163	DQ10_A	DQ10_B	256	B.DQ10						
A.DQ11	165	DQ11_A	DQ11_B	258	B.DQ11						
A.DQS1_P	22	DQS1_A_T	DQS1_B_T	115	B.DQS1_P						
A.DQS1_N	23	DQS1_A_C	DQS1_B_C	116	B.DQS1_N						
A.DQ12	25	DQ12_A	DQ12_B	118	B.DQ12						
A.DQ13	27	DQ13_A	DQ13_B	120	B.DQ13						
A.DQ14	170	DQ14_A	DQ14_B	263	B.DQ14						
A.DQ15	172	DQ15_A	DQ15_B	265	B.DQ15						
A.DQS6_P	168	DQS6_A_T	DQS6_B_T	261	B.DQS6_P						
A.DQS6_N	167	DQS6_A_C	DQS6_B_C	260	B.DQS6_N						
A.DQ16	29	DQ16_A	DQ16_B	122	B.DQ16						
A.DQ17	31	DQ17_A	DQ17_B	124	B.DQ17						
A.DQ18	174	DQ18_A	DQ18_B	267	B.DQ18						
A.DQ19	176	DQ19_A	DQ19_B	269	B.DQ19						
A.DQS2_P	33	DQS2_A_T	DQS2_B_T	126	B.DQS2_P						
A.DQS2_N	34	DQS2_A_C	DQS2_B_C	127	B.DQS2_N						
A.DQ20	36	DQ20_A	DQ20_B	129	B.DQ20						
A.DQ21	38	DQ21_A	DQ21_B	131	B.DQ21						
A.DQ22	181	DQ22_A	DQ22_B	274	B.DQ22						
A.DQ23	183	DQ23_A	DQ23_B	276	B.DQ23						
A.DQS7_P	179	DQS7_A_T	DQS7_B_T	272	B.DQS7_P						
A.DQS7_N	178	DQS7_A_C	DQS7_B_C	271	B.DQS7_N						
A.DQ24	40	DQ24_A	DQ24_B	133	B.DQ24						
A.DQ25	42	DQ25_A	DQ25_B	135	B.DQ25						
A.DQ26	185	DQ26_A	DQ26_B	278	B.DQ26						
A.DQ27	187	DQ27_A	DQ27_B	280	B.DQ27						
A.DQS3_P	44	DQS3_A_T	DQS3_B_T	137	B.DQS3_P						
A.DQS3_N	45	DQS3_A_C	DQS3_B_C	138	B.DQS3_N						
A.DQ28	47	DQ28_A	DQ28_B	140	B.DQ28						
A.DQ29	49	DQ29_A	DQ29_B	142	B.DQ29						
A.DQ30	192	DQ30_A	DQ30_B	285	B.DQ30						
A.DQ31	194	DQ31_A	DQ31_B	287	B.DQ31						
A.DQS8_P	190	DQS8_A_T	DQS8_B_T	283	B.DQS8_P						
A.DQS8_N	189	DQS8_A_C	DQS8_B_C	282	B.DQS8_N						
A.CB0	51	CB0_A	CB0_B	96	B.CB0						
A.CB1	53	CB1_A	CB1_B	98	B.CB1						
A.CB2	196	CB2_A	CB2_B	241	B.CB2						
A.CB3	198	CB3_A	CB3_B	243	B.CB3						
A.DQS4_P	55	DQS4_A_T	DQS4_B_T	239	B.DQS4_P						
A.DQS4_N	56	DQS4_A_C	DQS4_B_C	238	B.DQS4_N						
A.CB4	58	CB4_A	CB4_B	89	B.CB4						
A.CB5	60	CB5_A	CB5_B	91	B.CB5						
A.CB6	203	CB6_A	CB6_B	234	B.CB6						
A.CB7	205	CB7_A	CB7_B	236	B.CB7						
A.DQS9_P	201	DQS9_A_T	DQS9_B_T	93	B.DQS9_P						
A.DQS9_N	200	DQS9_A_C	DQS9_B_C	94	B.DQS9_N						

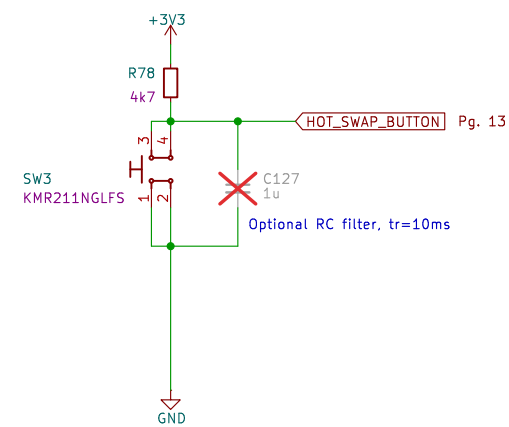
Power, address command and control



HOT SWAP status LED

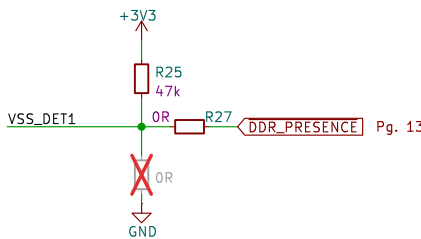


HOT SWAP eject button

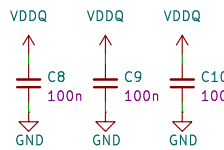


RDIMM detect

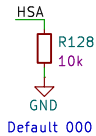
	Populated	Not populated
DDR_PRESENCE	0	1



Plane decoupling



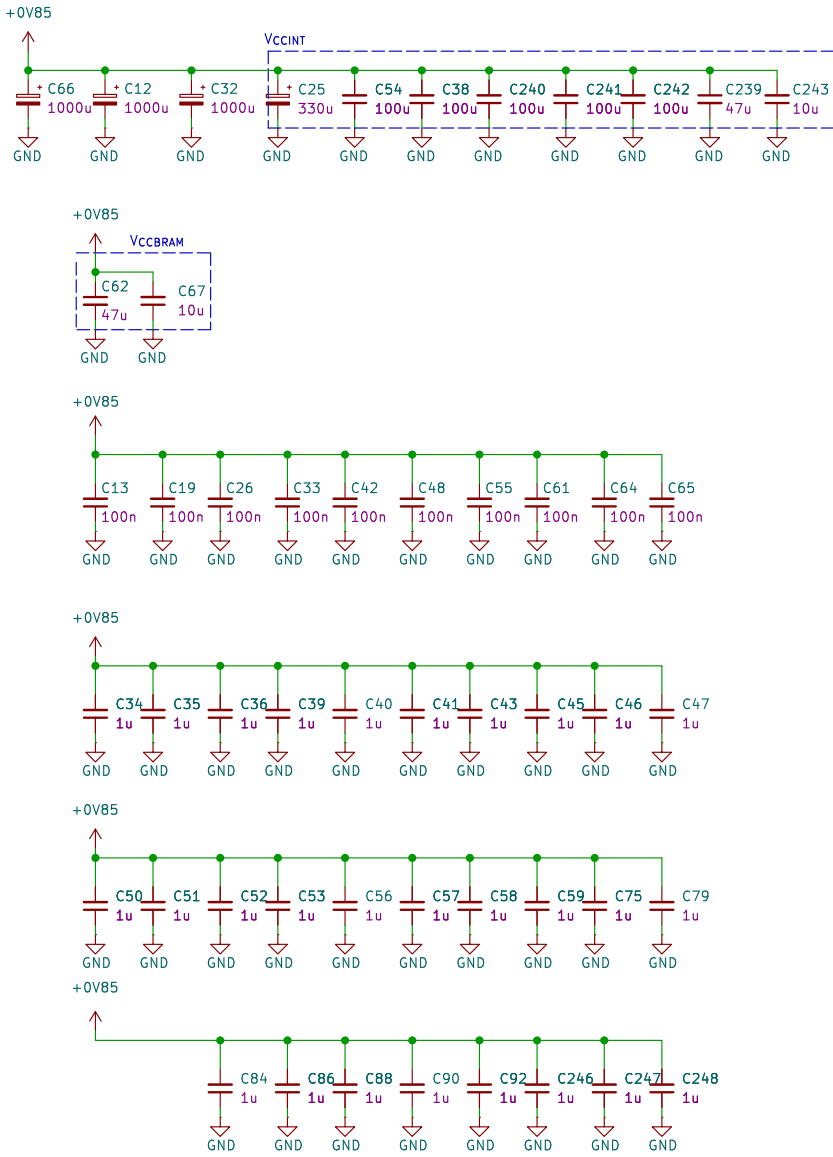
Serial address select



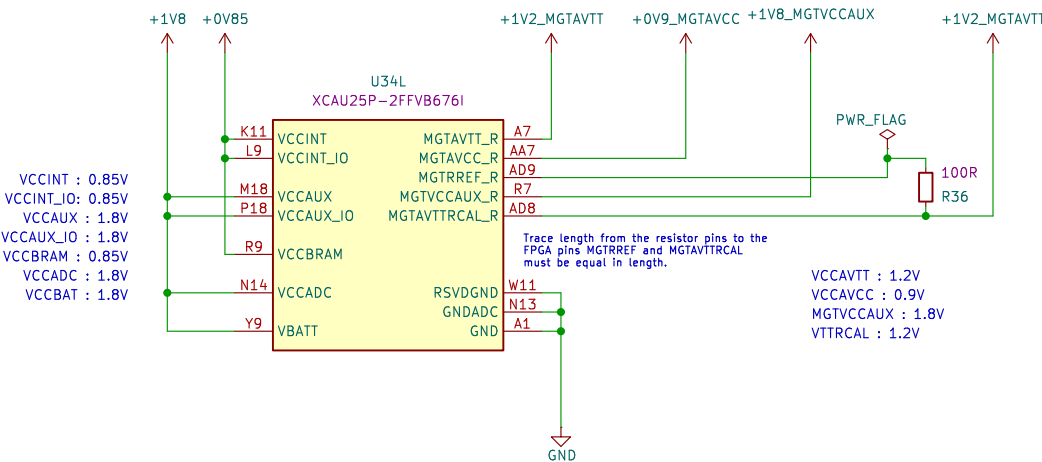
FPGA Power rails

Bank marked by dashed line
referenced from US+ Series FGAs
PCB Design Guide UG583
(AUP25P+ XCKU5P FFVB Package worst case)
MGT decoupling marked by dahed line
referenced from US+ Series FGAs
PCB Design Guide UG576
(AUP25P+ XCKU5P FFVB Package worst case)

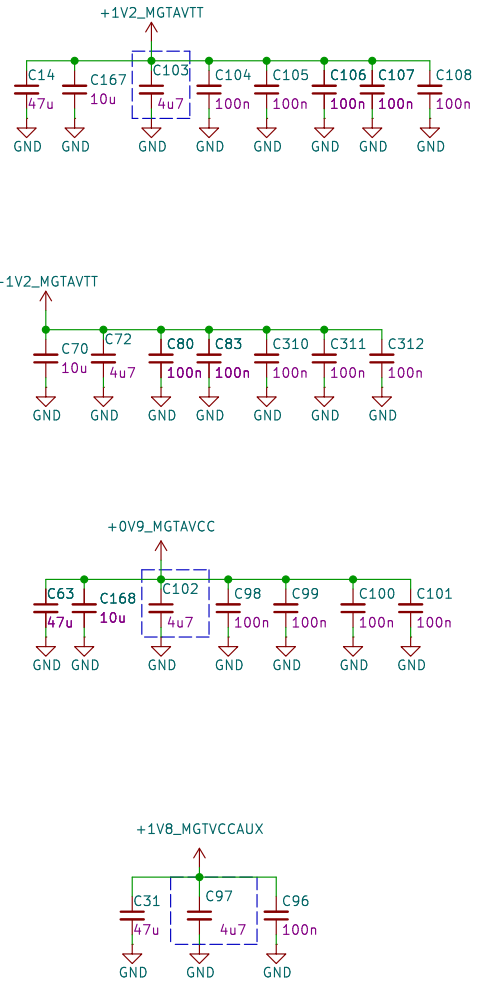
VCCINT decoupling



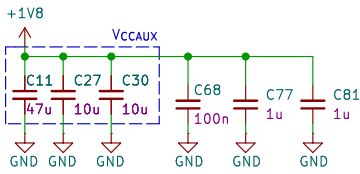
FPGA



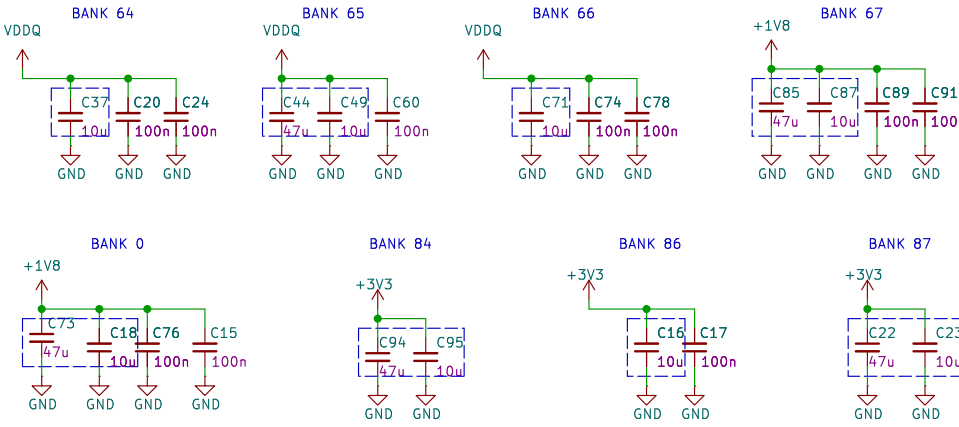
MGT decoupling



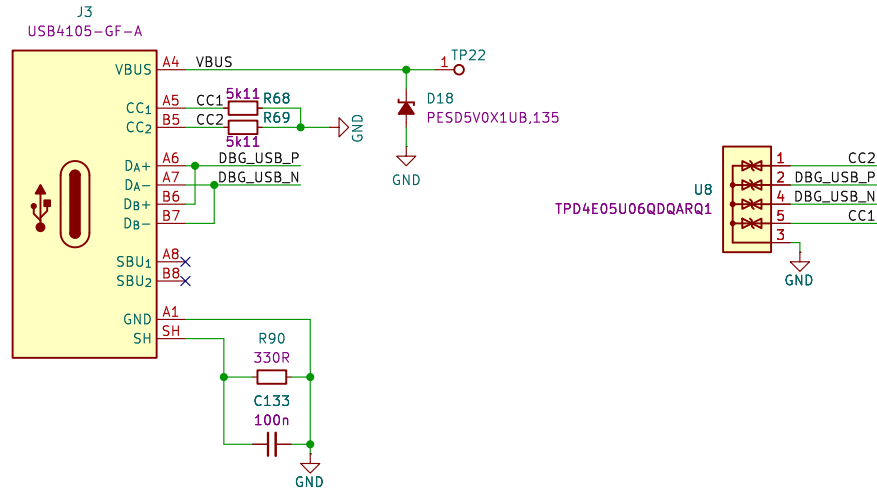
VCCINT decoupling



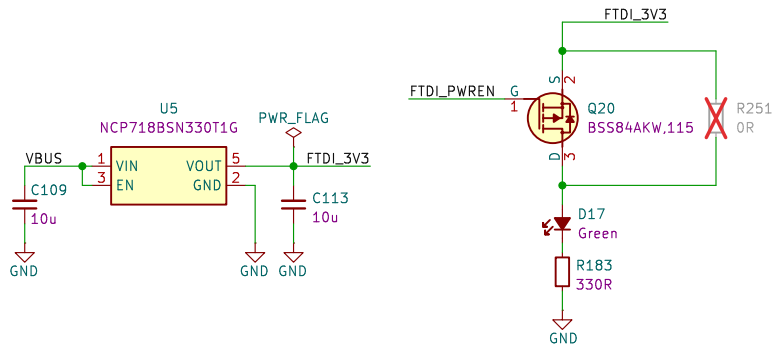
Bank decoupling



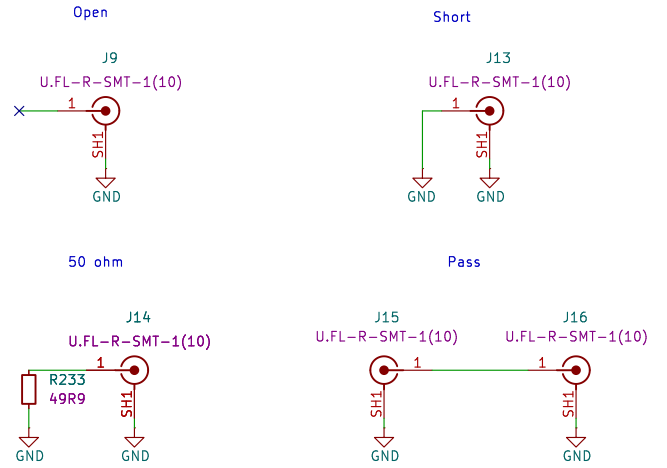
Debug FTDI
USB-C



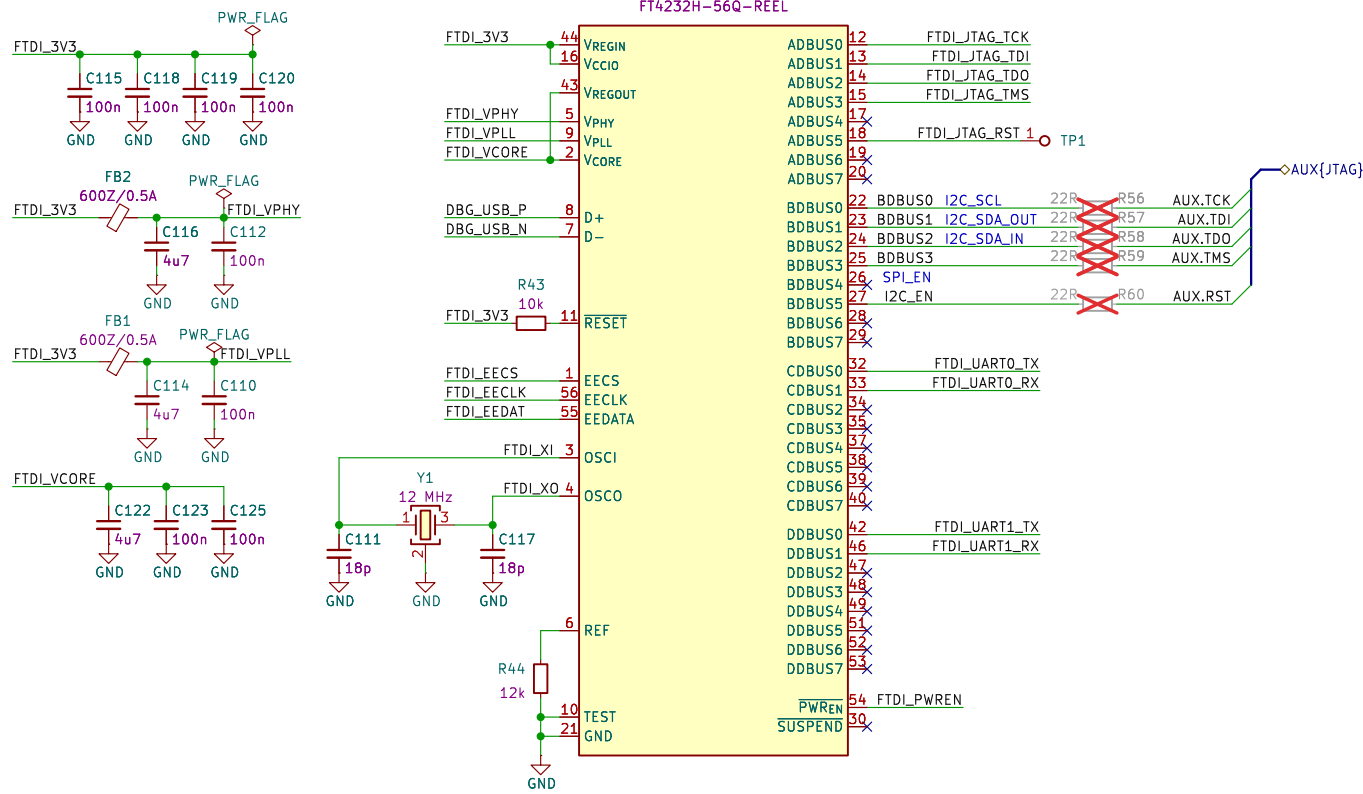
LDO



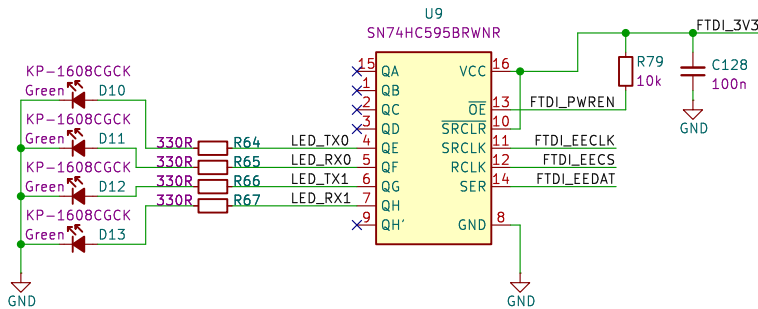
VNA calibration



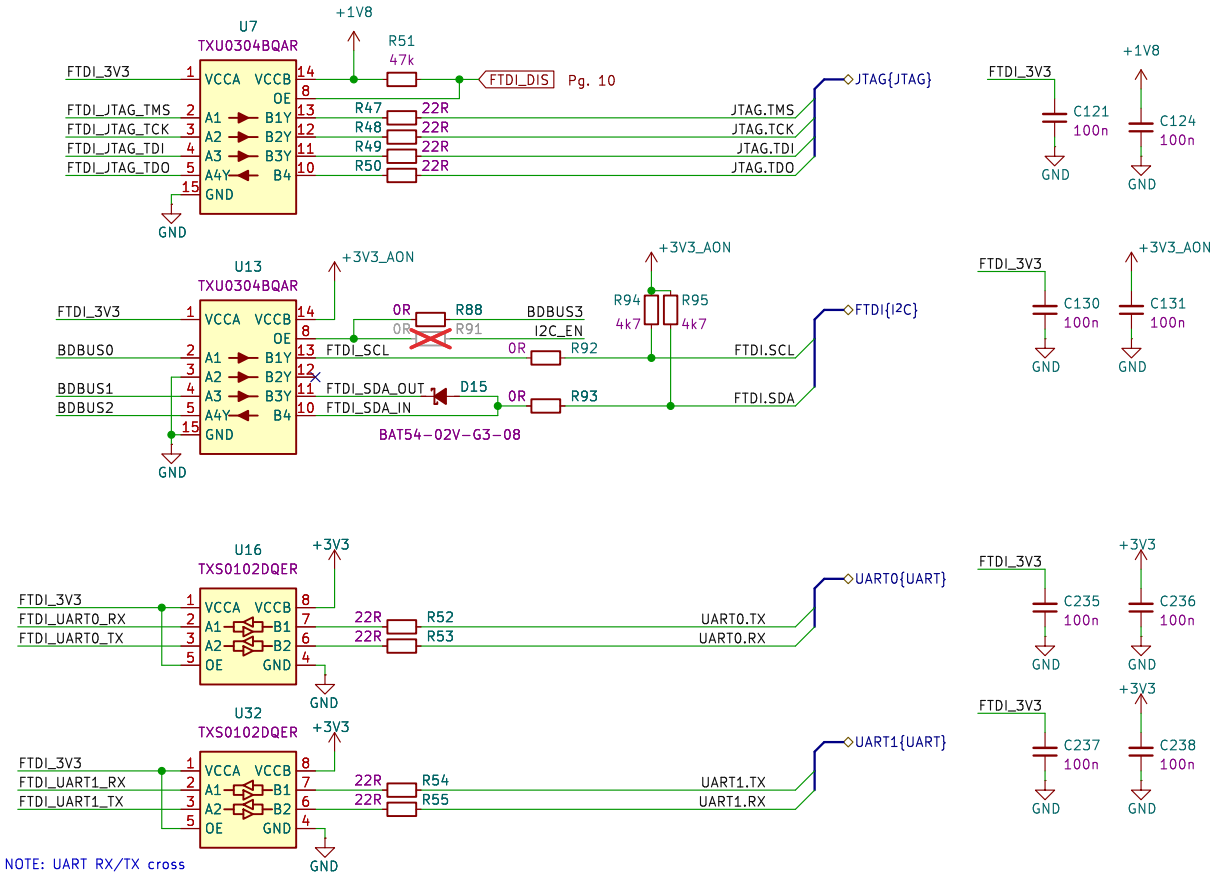
FTDI



Shift register



Logic level translators

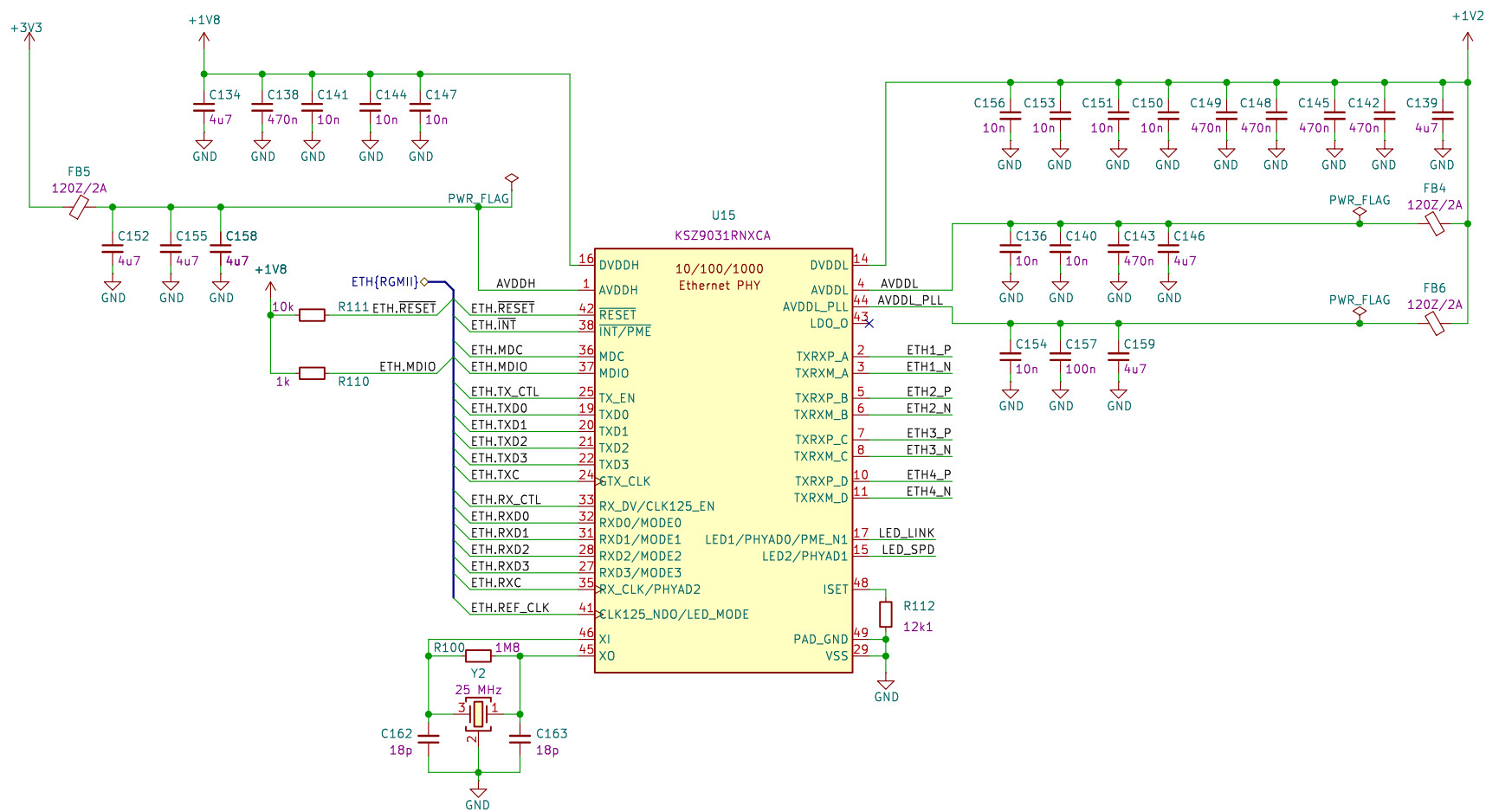


NOTE: UART RX/TX cross

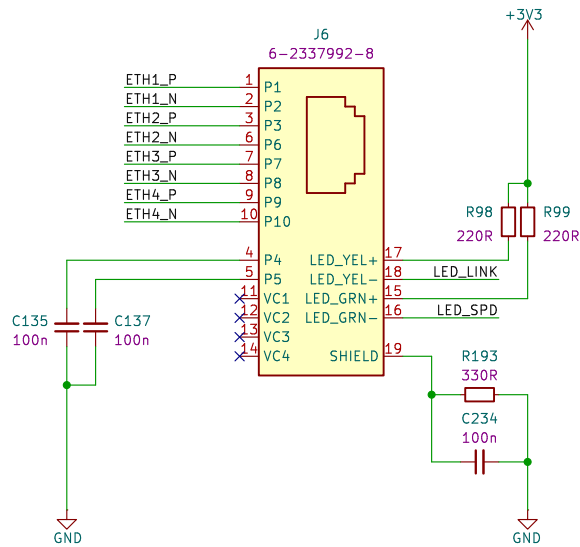


Gigabit Ethernet

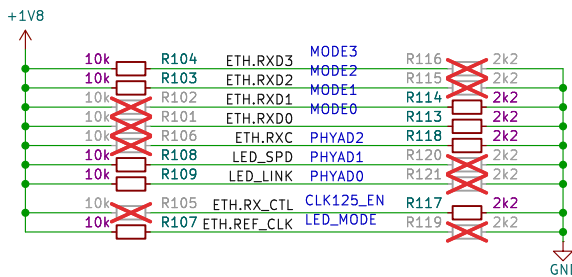
Ethernet PHY



RJ45 connector

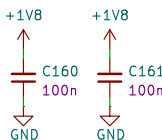


Bootstrap configuration



MODE[3:0] : 1100 (RGMII mode - Advertise 1000BASE-T full-duplex only)
PHYAD[4:0] : 00011
CLK125_EN : 0, disabled
LED_MODE : 1, Single-LED mode

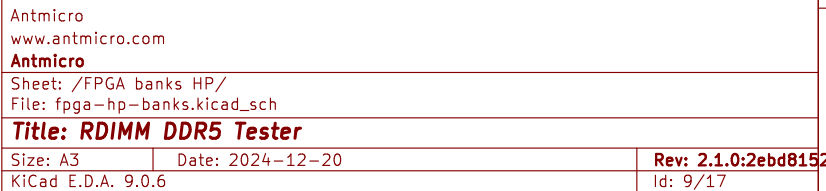
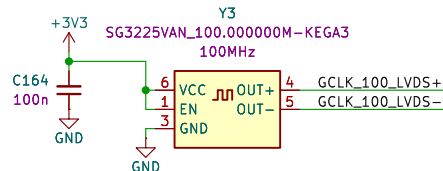
Reference plane decoupling



VCC0 (HP banks) max: 1.9V

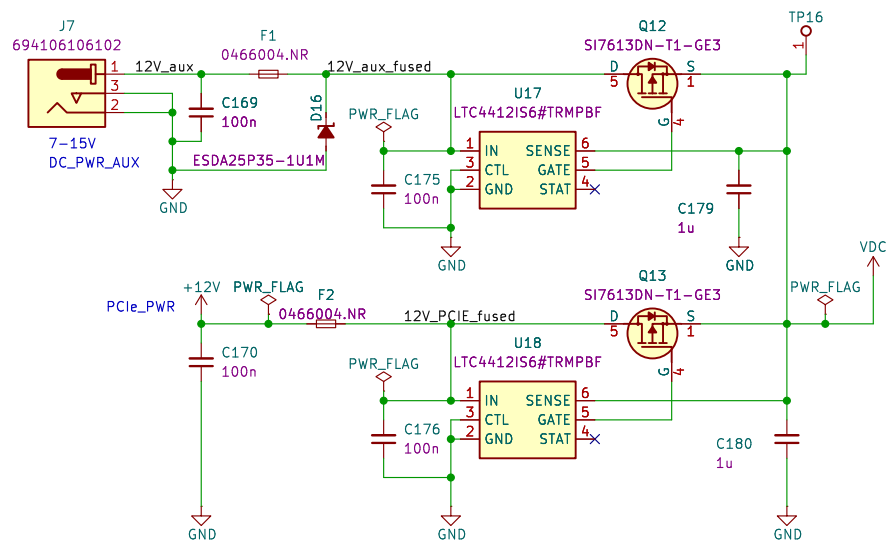


Clock source

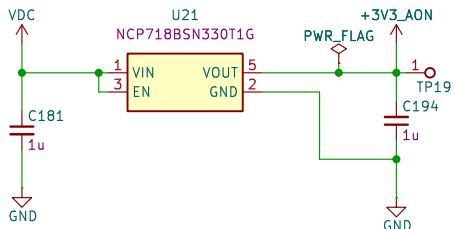


Power supply

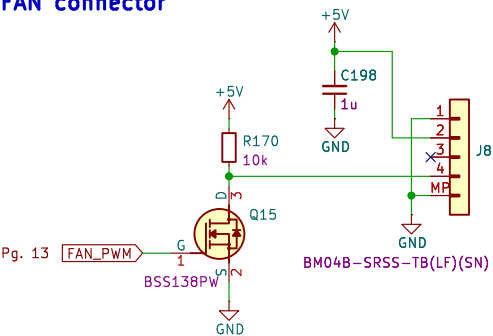
Power source



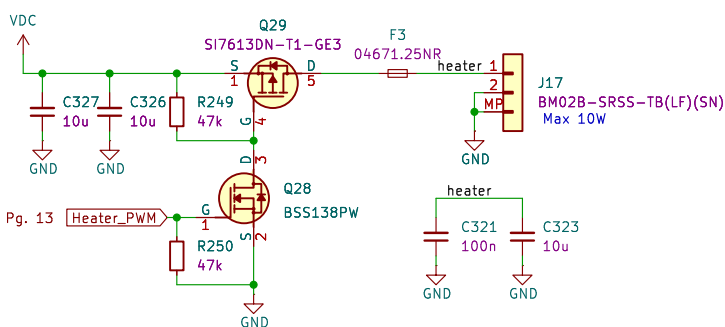
Always-ON +3V3 LDO



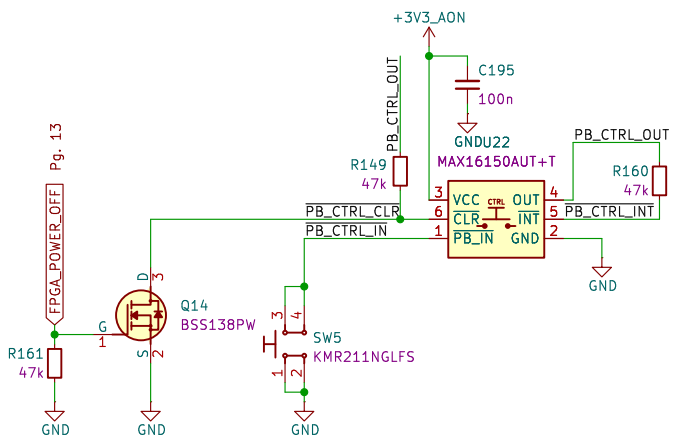
FAN connector



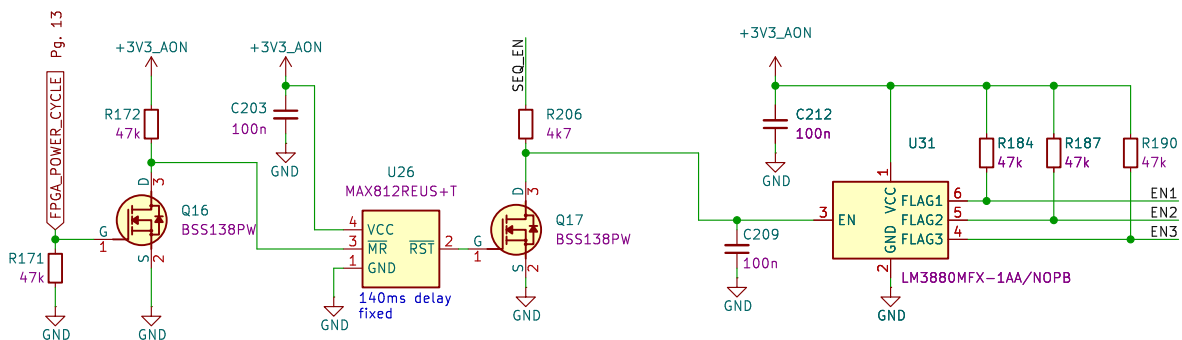
Heater connector



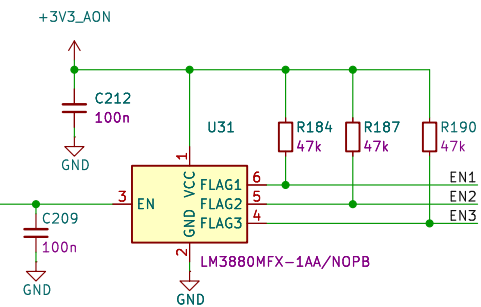
ON/OFF Button controller



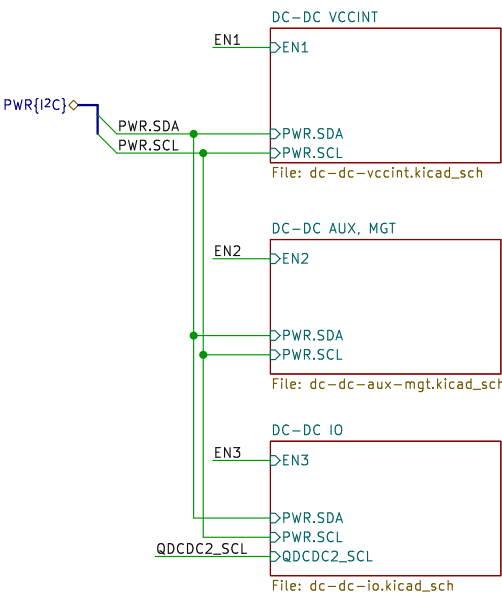
Power cycle



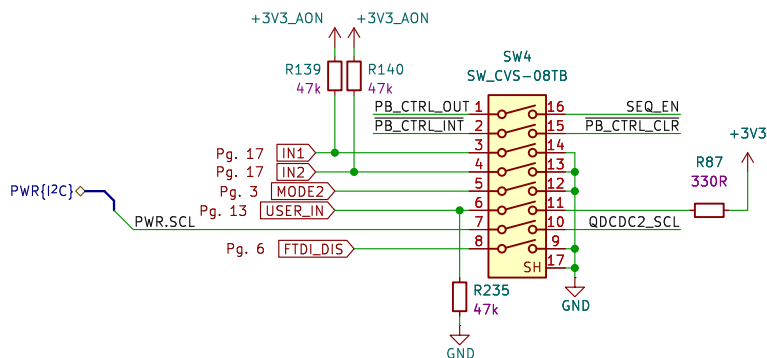
Power supply sequencer



DC-DCs

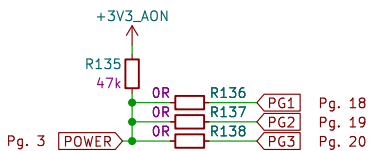


Config switch

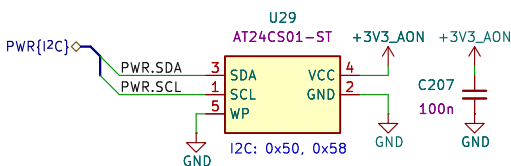


- NOTE:
1. AUTO ON/ PB-Controller
 2. 8s off/ instant off
 3. PWR I2C MUX input select 1
 4. PWR I2C MUX input select 2
 5. JTAG/SPI FLASH
 6. USER_IN
 7. Connect QDCDC2_I2C
 8. Disable FTDI JTAG

Power good



UID



Ground probe pads



Antmicro
www.antmicro.com

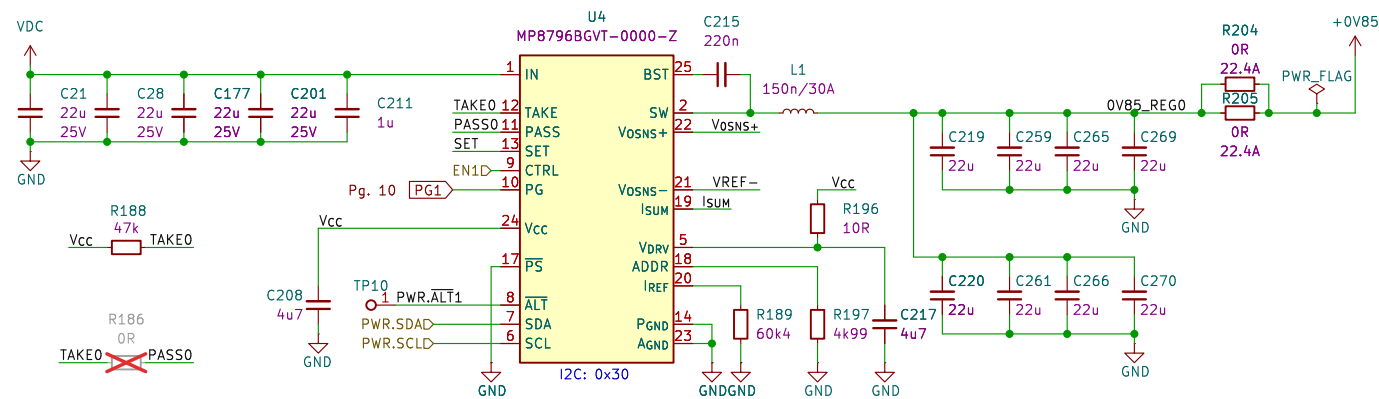
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Title: RDIMM DDR5 Tester

Size: A3 Date: 2024-12-20
KiCad E.D.A. 9.0.6

Rev: 2.1.0:2ebd8152
Id: 10/17

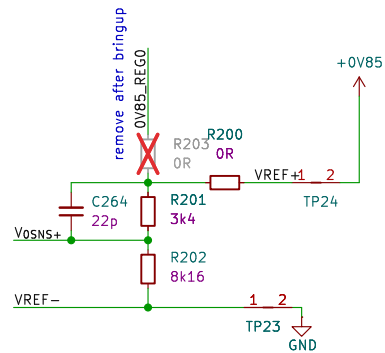
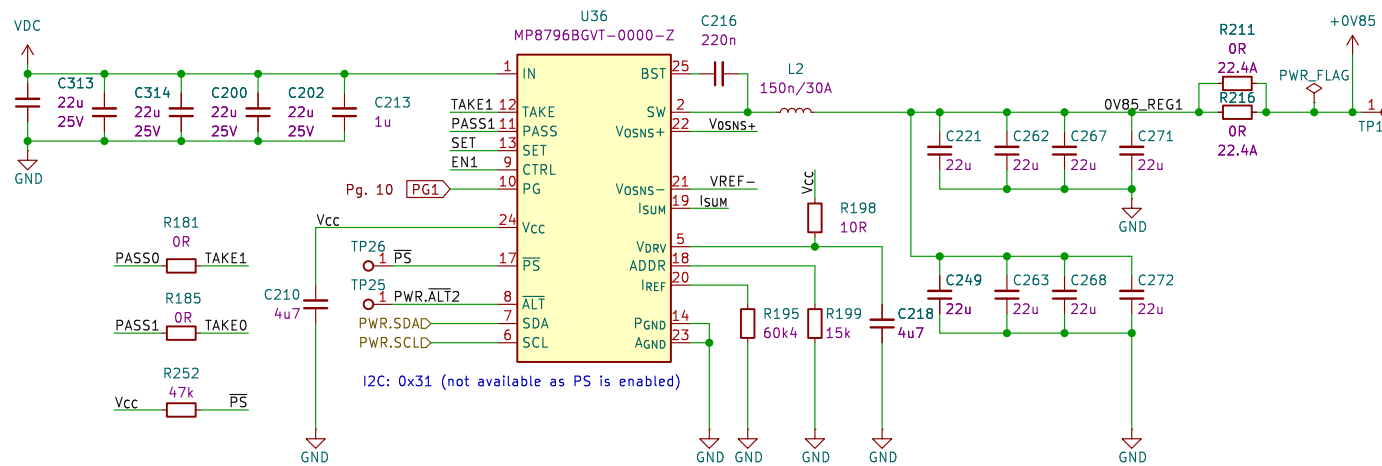
DC-DC INT



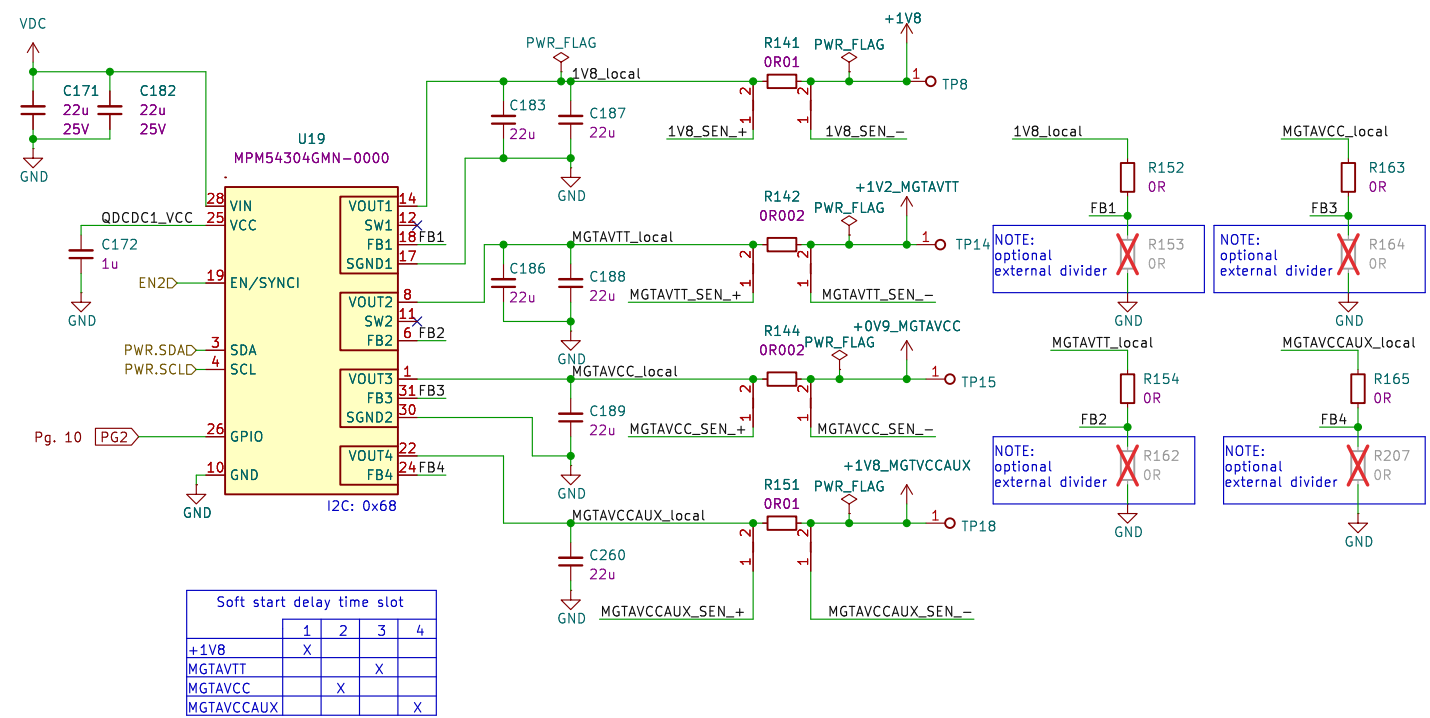
MP8796BGVT-0000-Z selected due to its wide availability on the market
Replace with MPQ8655GVT when it becomes available on the market

Pin compatible PN: MPQ8645P, MPQ8655GVT

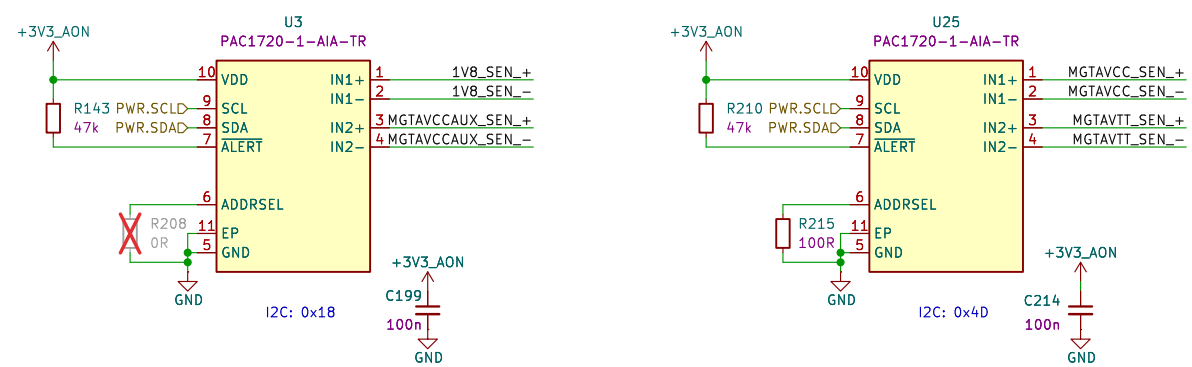
Second phase is for VCCINT > 20A applications
Do Not Populate if not required
(place R188 instead)



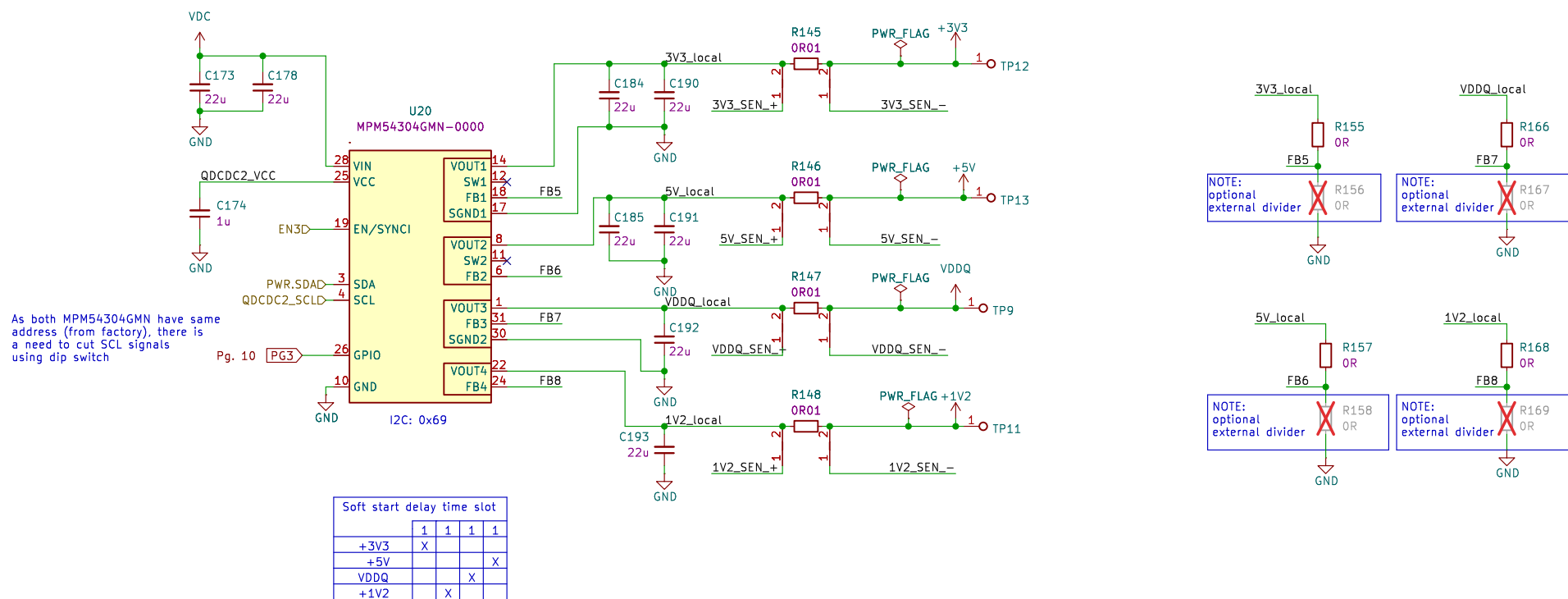
DC-DC AUX, MGT



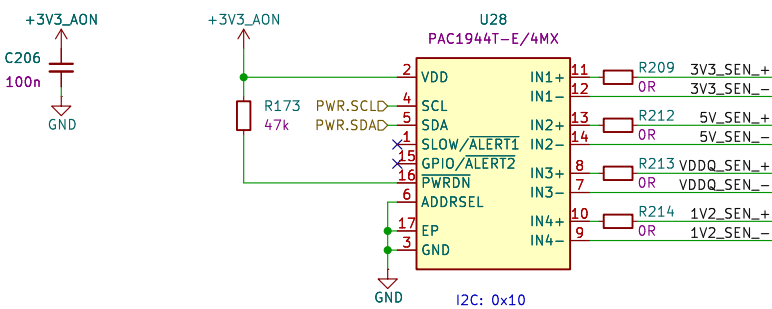
Current sense monitors



DC-DC IO



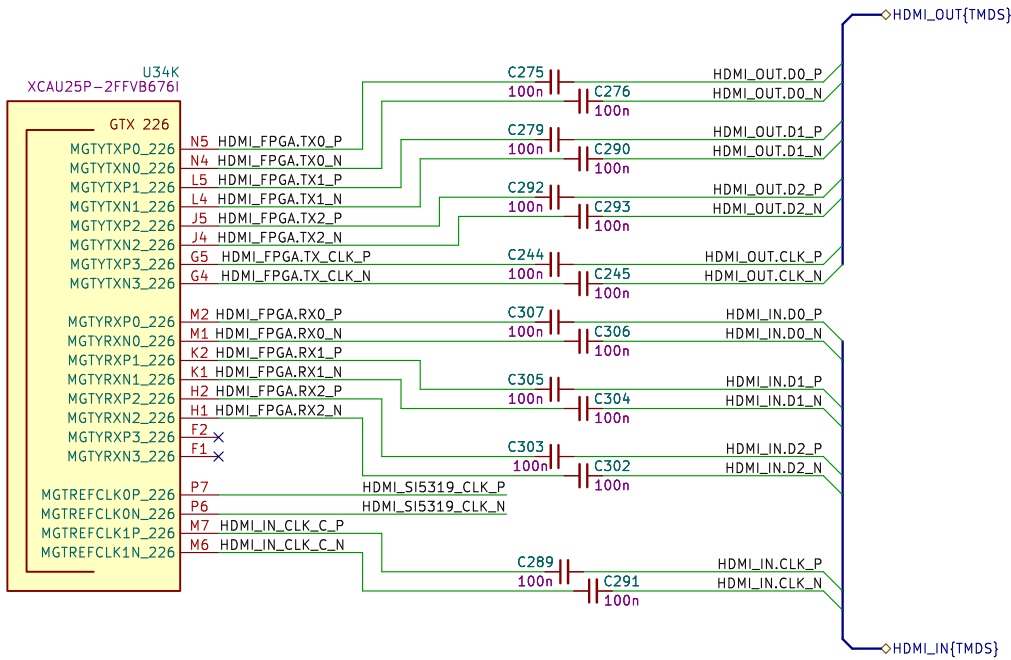
Current sense monitor



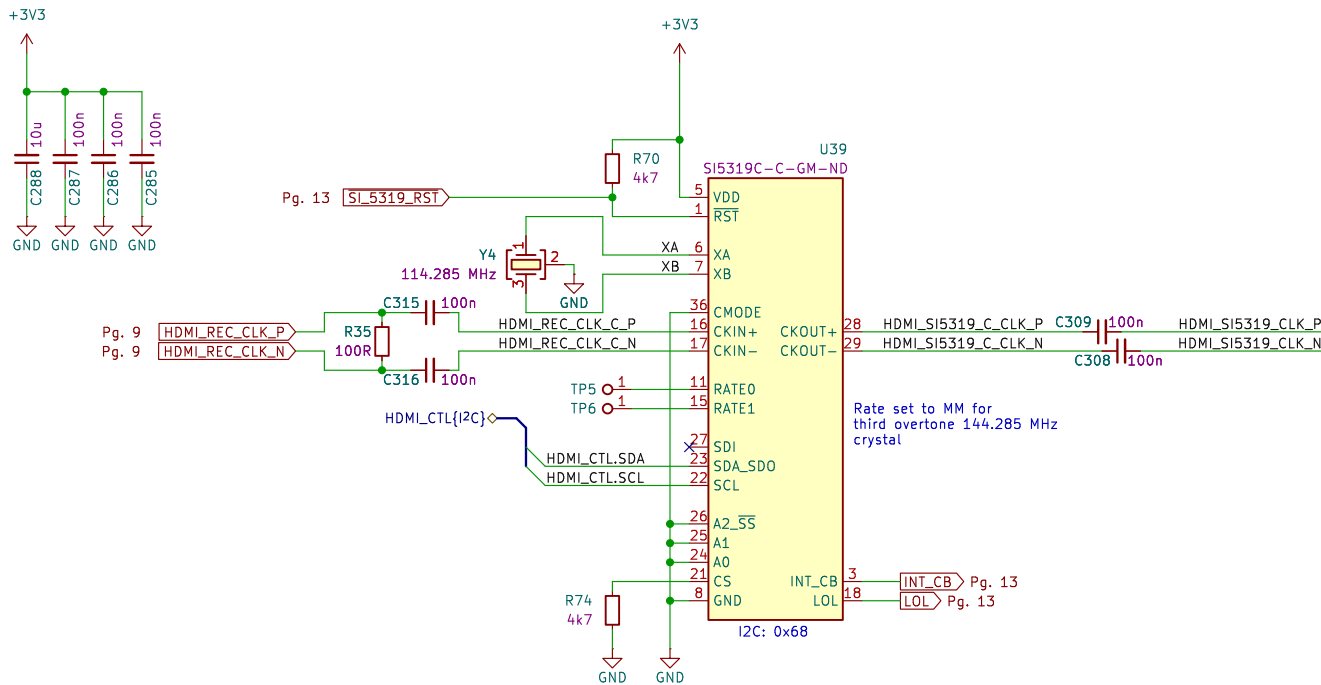
MGT Interface
PCIe 3.0 x8



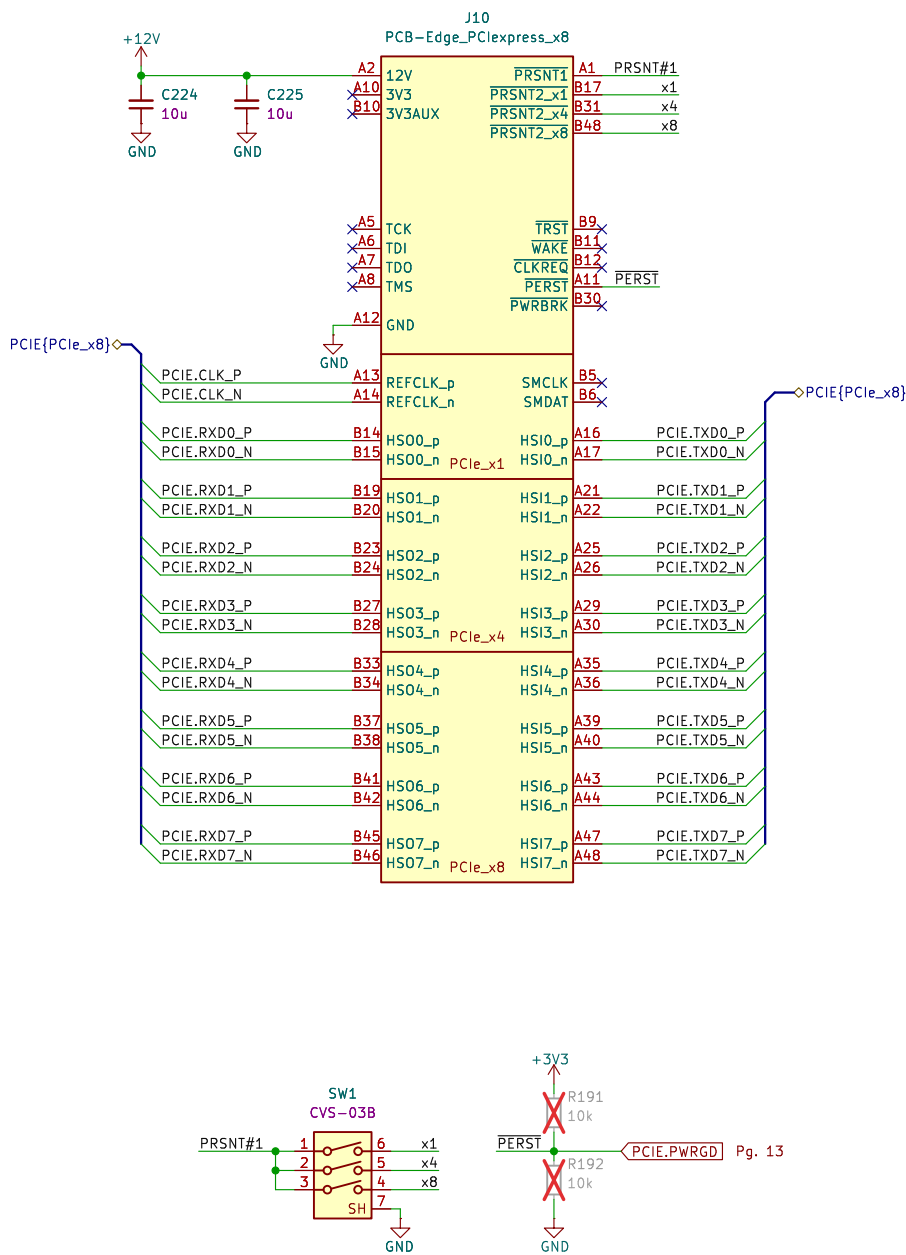
HDMI



Clock multiplier



PCIe



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Antmicro

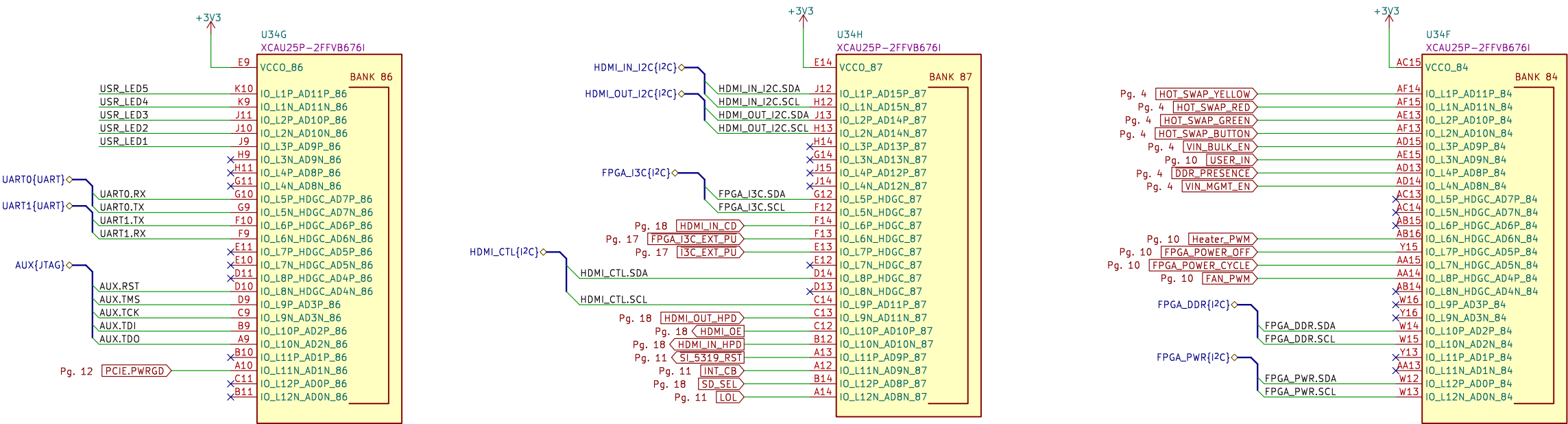
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Title: **RDIMM DDR5 Tester**

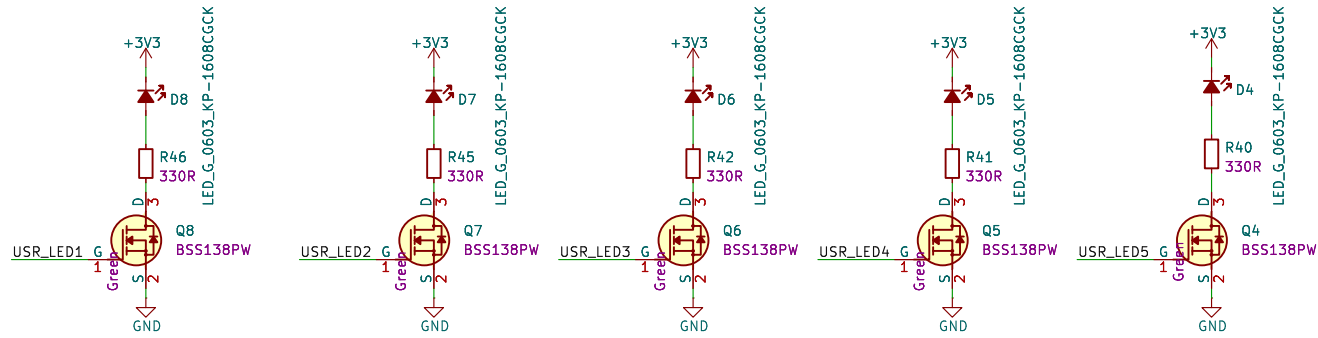
Size: A3 Date: 2024-12-20
KiCad E.D.A. 9.0.6

Rev: **2.1.0:2ebd8152**
Id: 12/17

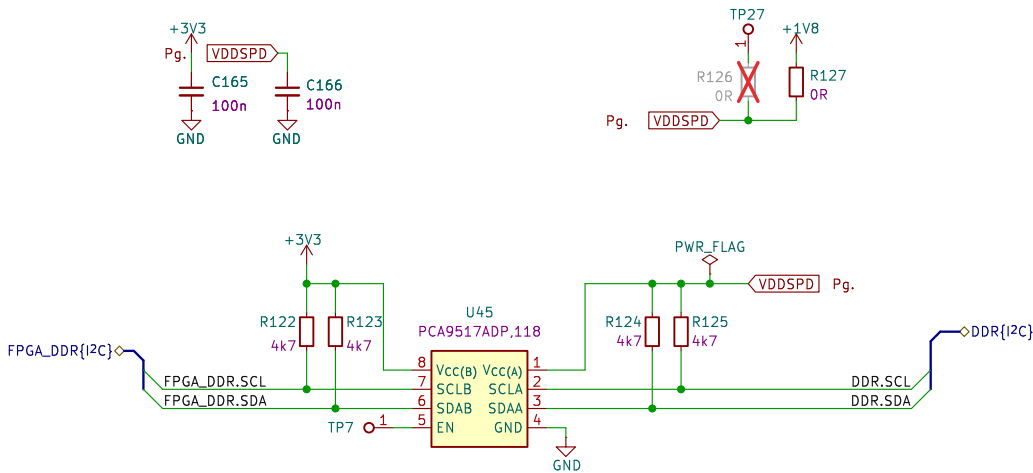
BANKS HD



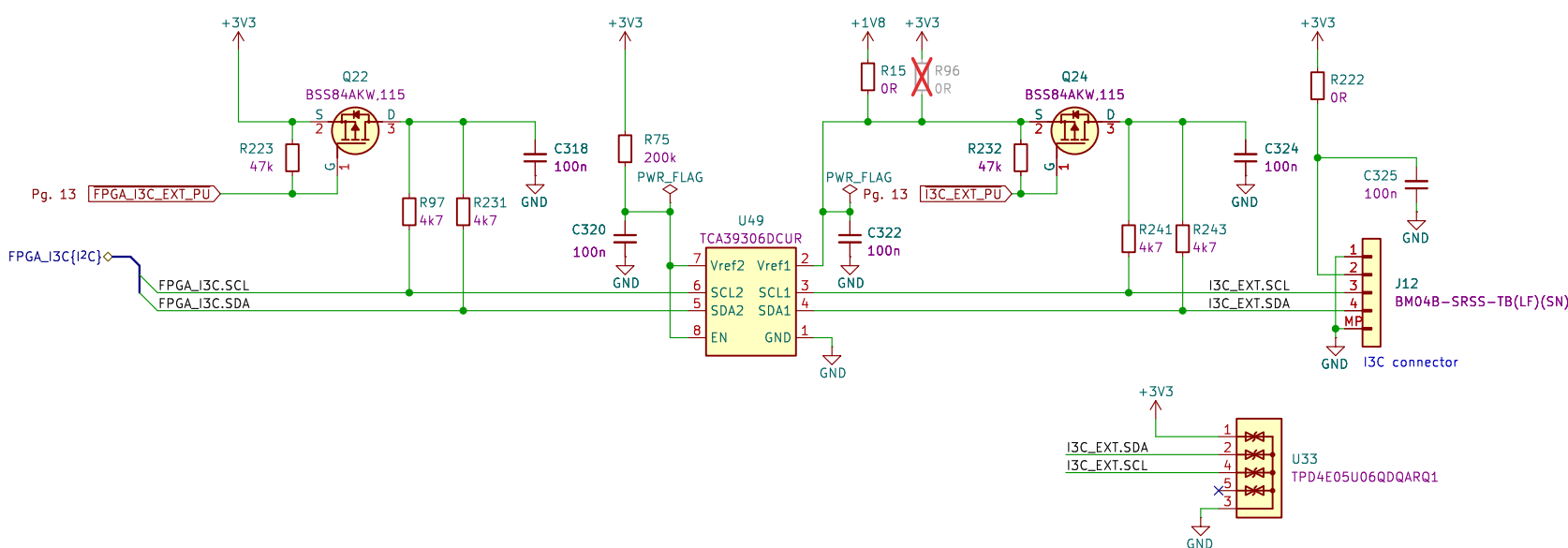
User LEDs



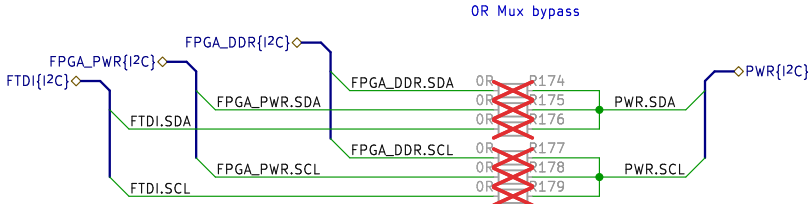
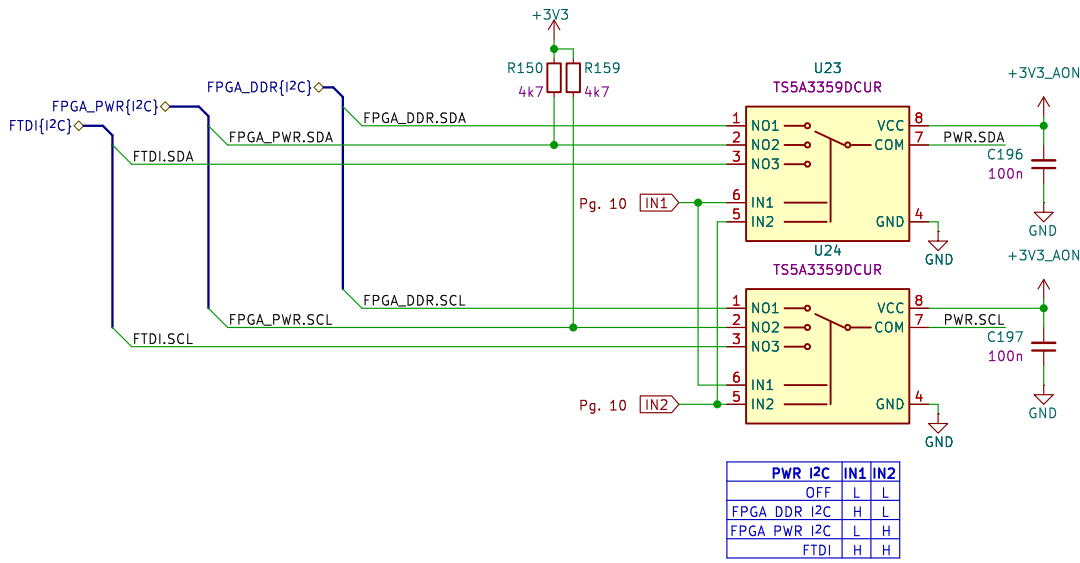
I2C



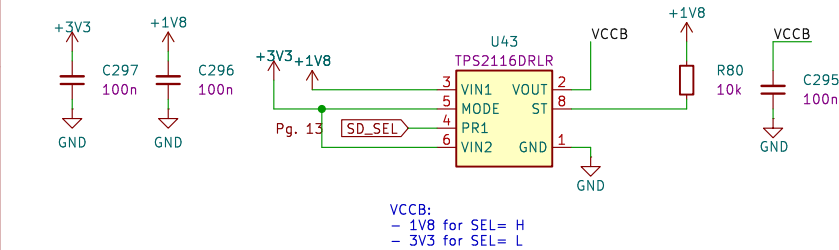
I3C



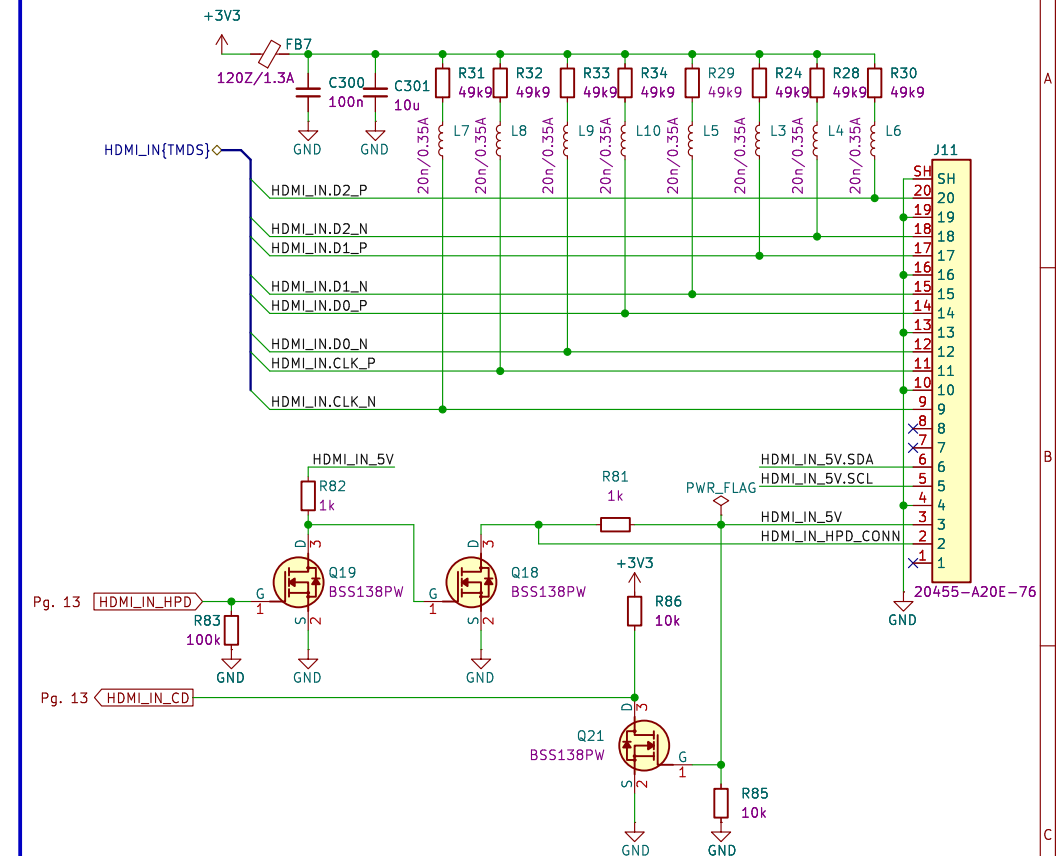
PWR I2C MUX



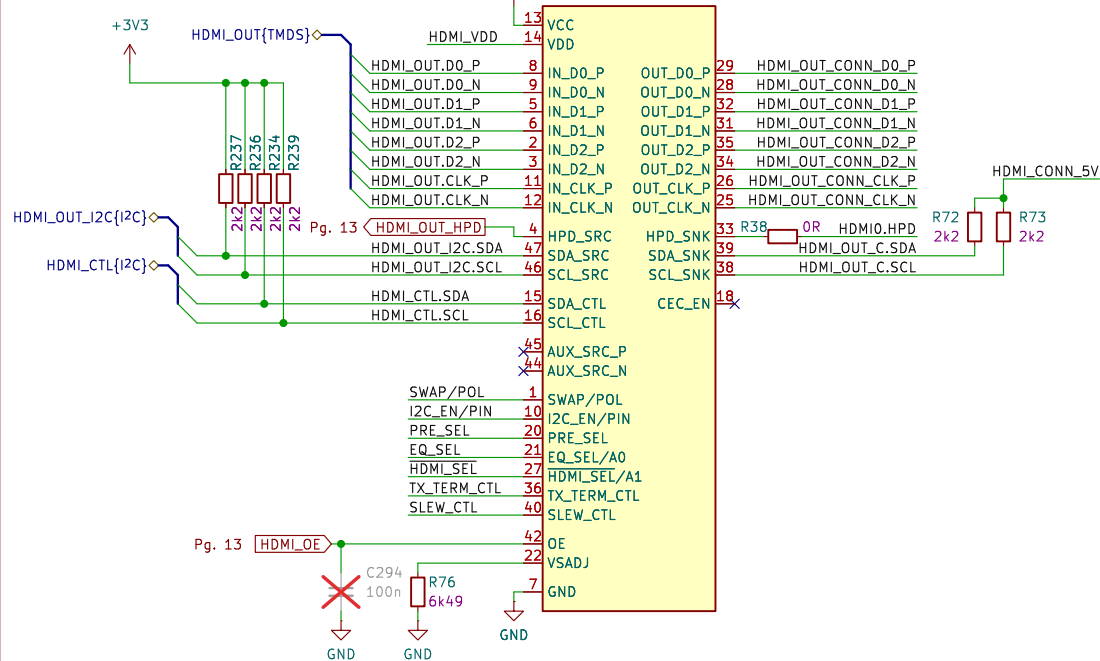
Voltage level translator



HDMI input connector



HDMI retimer



The diagrams show the following connections for each component:

- U37:**
 - Pin 1: HDMI_IN.D2_P
 - Pin 2: HDMI_IN.D2_N
 - Pin 4: HDMI_IN.D1_P
 - Pin 5: HDMI_IN.D1_N
 - Pin 3: GND
- U41:**
 - Pin 1: HDMI_IN.DO_P
 - Pin 2: HDMI_IN.DO_N
 - Pin 4: HDMI_IN.CLK_P
 - Pin 5: HDMI_IN.CLK_N
 - Pin 3: GND
- U47:**
 - Pin 1: HDMI_IN_5V.SDA
 - Pin 2: HDMI_IN_5V.SCL
 - Pin 4: HDMI_IN_5V
 - Pin 5: HDMI_IN_HPD_CONN
 - Pin 3: GND

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[illegible]