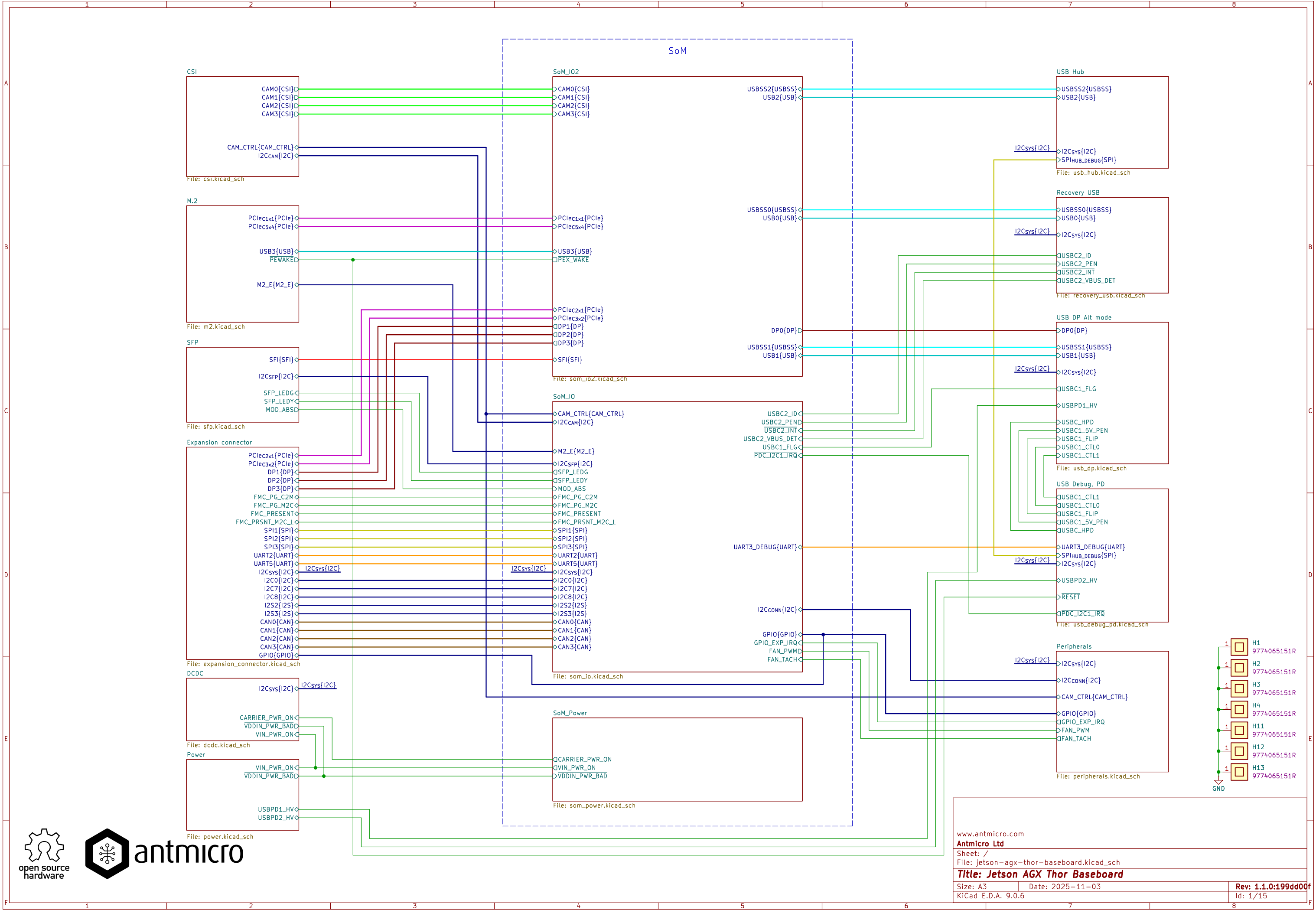




The diagram illustrates the connection of various components to a central processor (J1C, J1B, J1E, J1F) through a SOM (System on Module). The components are connected via USB, PCIe, DP, and CSI interfaces.

USB Connections:

- USB0{USB}:** USB0.D+, USB0.D-, USB0.N
- USB1{USB}:** USB1.D+, USB1.D-, USB1.N
- USB2{USB}:** USB2.D+, USB2.D-, USB2.N
- USB3{USB}:** USB3.D+, USB3.D-, USB3.N
- USBSS0{USBSS}:** USBSS0.TX+, USBSS0.TX-, USBSS0.RX+, USBSS0.RX-
- USBSS1{USBSS}:** USBSS1.TX+, USBSS1.TX-, USBSS1.RX+, USBSS1.RX-
- USBSS2{USBSS}:** USBSS2.TX+, USBSS2.TX-, USBSS2.RX+, USBSS2.RX-

PCIe Connections:

- PCIEC2x1{PCIE}:** PCIEC2x1.RST, PCIEC2x1.CLKREQ, PCIEC2x1.CLK+, PCIEC2x1.CLK-
- PCIEC1x1{PCIE}:** PCIEC1x1.RST, PCIEC1x1.CLKREQ, PCIEC1x1.CLK+, PCIEC1x1.CLK-
- PCIEC5x4{PCIE}:** PCIEC5x4.RST, PCIEC5x4.CLKREQ, PCIEC5x4.CLK+, PCIEC5x4.CLK-
- PCIEC3x2{PCIE}:** PCIEC3x2.RST, PCIEC3x2.CLKREQ, PCIEC3x2.CLK+, PCIEC3x2.CLK-
- SFI{SFI}:** SFI.TX+, SFI.TX-, SFI.RX+, SFI.RX-

DP and CSI Connections:

- DP0{DP}:** DP0.TX0+, DP0.TX0-, DP0.TX1+, DP0.TX1-, DP0.TX2+, DP0.TX2-, DP0.TX3+, DP0.TX3-, DP0.HPD, DP0.AUX+, DP0.AUX-
- DP1{DP}:** DP1.TX0+, DP1.TX0-, DP1.TX1+, DP1.TX1-, DP1.TX2+, DP1.TX2-, DP1.TX3+, DP1.TX3-, DP1.HPD, DP1.AUX+, DP1.AUX-
- DP2{DP}:** DP2.TX0+, DP2.TX0-, DP2.TX1+, DP2.TX1-, DP2.TX2+, DP2.TX2-, DP2.TX3+, DP2.TX3-, DP2.HPD, DP2.AUX+, DP2.AUX-
- DP3{DP}:** DP3.TX0+, DP3.TX0-, DP3.TX1+, DP3.TX1-, DP3.TX2+, DP3.TX2-, DP3.TX3+, DP3.TX3-, DP3.HPD, DP3.AUX+, DP3.AUX-
- CAM1{CSI}:** CAM1.CSI0.CLK+, CAM1.CSI0.CLK-, CAM1.CSI0.D0+, CAM1.CSI0.D0-, CAM1.CSI0.D1+, CAM1.CSI0.D1-, CAM1.CSI1.D0+, CAM1.CSI1.D0-, CAM1.CSI1.D1+, CAM1.CSI1.D1-
- CAM2{CSI}:** CAM2.CSI4.CLK+, CAM2.CSI4.CLK-, CAM2.CSI4.D0+, CAM2.CSI4.D0-, CAM2.CSI4.D1+, CAM2.CSI4.D1-, CAM2.CSI5.D0+, CAM2.CSI5.D0-, CAM2.CSI5.D1+, CAM2.CSI5.D1-
- CAM3{CSI}:** CAM3.CSI6.CLK+, CAM3.CSI6.CLK-, CAM3.CSI6.D0+, CAM3.CSI6.D0-, CAM3.CSI6.D1+, CAM3.CSI6.D1-, CAM3.CSI7.D0+, CAM3.CSI7.D0-, CAM3.CSI7.D1+, CAM3.CSI7.D1-

Other Connections:

- UPHY0:** UPHY_RX0_P, UPHY_RX0_N, UPHY_RX1_P, UPHY_RX1_N, UPHY_RX2_P, UPHY_RX2_N, UPHY_RX3_P, UPHY_RX3_N, UPHY_RX4_P, UPHY_RX4_N, UPHY_RX5_P, UPHY_RX5_N, UPHY_RX6_P, UPHY_RX6_N, UPHY_RX7_P, UPHY_RX7_N
- UPHY1:** UPHY_RX8_P, UPHY_RX8_N, UPHY_RX9_P, UPHY_RX9_N, UPHY_RX10_P, UPHY_RX10_N, UPHY_RX11_P, UPHY_RX11_N, UPHY_RX12_P, UPHY_RX12_N, UPHY_RX13_P, UPHY_RX13_N, UPHY_RX14_P, UPHY_RX14_N, UPHY_RX15_P, UPHY_RX15_N, UPHY_RX16_P, UPHY_RX16_N
- UPHY2:** UPHY_TX0_P, UPHY_TX0_N, UPHY_TX1_P, UPHY_TX1_N, UPHY_TX2_P, UPHY_TX2_N, UPHY_TX3_P, UPHY_TX3_N, UPHY_TX4_P, UPHY_TX4_N, UPHY_TX5_P, UPHY_TX5_N, UPHY_TX6_P, UPHY_TX6_N, UPHY_TX7_P, UPHY_TX7_N
- UPHY3:** UPHY_TX8_P, UPHY_TX8_N, UPHY_TX9_P, UPHY_TX9_N, UPHY_TX10_P, UPHY_TX10_N, UPHY_TX11_P, UPHY_TX11_N, UPHY_TX12_P, UPHY_TX12_N, UPHY_TX13_P, UPHY_TX13_N, UPHY_TX14_P, UPHY_TX14_N, UPHY_TX15_P, UPHY_TX15_N, UPHY_TX16_P, UPHY_TX16_N

The diagram illustrates the connection of various components to a central processor (J1C, J1B, J1E, J1F) through a SOM (System on Module). The components are connected via USB, PCIe, DP, and CSI interfaces.

USB Connections:

- USB0{USB}:** USB0.D+, USB0.D-, USB0.N
- USB1{USB}:** USB1.D+, USB1.D-, USB1.N
- USB2{USB}:** USB2.D+, USB2.D-, USB2.N
- USB3{USB}:** USB3.D+, USB3.D-, USB3.N
- USBSS0{USBSS}:** USBSS0.TX+, USBSS0.TX-, USBSS0.RX+, USBSS0.RX-
- USBSS1{USBSS}:** USBSS1.TX+, USBSS1.TX-, USBSS1.RX+, USBSS1.RX-
- USBSS2{USBSS}:** USBSS2.TX+, USBSS2.TX-, USBSS2.RX+, USBSS2.RX-

PCIe Connections:

- PCIEC2x1{PCIE}:** PCIEC2x1.RST, PCIEC2x1.CLKREQ, PCIEC2x1.CLK+, PCIEC2x1.CLK-
- PCIEC1x1{PCIE}:** PCIEC1x1.RST, PCIEC1x1.CLKREQ, PCIEC1x1.CLK+, PCIEC1x1.CLK-
- PCIEC5x4{PCIE}:** PCIEC5x4.RST, PCIEC5x4.CLKREQ, PCIEC5x4.CLK+, PCIEC5x4.CLK-
- PCIEC3x2{PCIE}:** PCIEC3x2.RST, PCIEC3x2.CLKREQ, PCIEC3x2.CLK+, PCIEC3x2.CLK-
- SFI{SFI}:** SFI.TX+, SFI.TX-, SFI.RX+, SFI.RX-

DP and CSI Connections:

- DP0{DP}:** DP0.TX0+, DP0.TX0-, DP0.TX1+, DP0.TX1-, DP0.TX2+, DP0.TX2-, DP0.TX3+, DP0.TX3-, DP0.HPD, DP0.AUX+, DP0.AUX-
- DP1{DP}:** DP1.TX0+, DP1.TX0-, DP1.TX1+, DP1.TX1-, DP1.TX2+, DP1.TX2-, DP1.TX3+, DP1.TX3-, DP1.HPD, DP1.AUX+, DP1.AUX-
- DP2{DP}:** DP2.TX0+, DP2.TX0-, DP2.TX1+, DP2.TX1-, DP2.TX2+, DP2.TX2-, DP2.TX3+, DP2.TX3-, DP2.HPD, DP2.AUX+, DP2.AUX-
- DP3{DP}:** DP3.TX0+, DP3.TX0-, DP3.TX1+, DP3.TX1-, DP3.TX2+, DP3.TX2-, DP3.TX3+, DP3.TX3-, DP3.HPD, DP3.AUX+, DP3.AUX-
- CAM1{CSI}:** CAM1.CSI0.CLK+, CAM1.CSI0.CLK-, CAM1.CSI0.D0+, CAM1.CSI0.D0-, CAM1.CSI0.D1+, CAM1.CSI0.D1-, CAM1.CSI1.D0+, CAM1.CSI1.D0-, CAM1.CSI1.D1+, CAM1.CSI1.D1-
- CAM2{CSI}:** CAM2.CSI4.CLK+, CAM2.CSI4.CLK-, CAM2.CSI4.D0+, CAM2.CSI4.D0-, CAM2.CSI4.D1+, CAM2.CSI4.D1-, CAM2.CSI5.D0+, CAM2.CSI5.D0-, CAM2.CSI5.D1+, CAM2.CSI5.D1-
- CAM3{CSI}:** CAM3.CSI6.CLK+, CAM3.CSI6.CLK-, CAM3.CSI6.D0+, CAM3.CSI6.D0-, CAM3.CSI6.D1+, CAM3.CSI6.D1-, CAM3.CSI7.D0+, CAM3.CSI7.D0-, CAM3.CSI7.D1+, CAM3.CSI7.D1-

Other Connections:

- UPHY0:** UPHY_RX0_P, UPHY_RX0_N, UPHY_RX1_P, UPHY_RX1_N, UPHY_RX2_P, UPHY_RX2_N, UPHY_RX3_P, UPHY_RX3_N, UPHY_RX4_P, UPHY_RX4_N, UPHY_RX5_P, UPHY_RX5_N, UPHY_RX6_P, UPHY_RX6_N, UPHY_RX7_P, UPHY_RX7_N
- UPHY1:** UPHY_RX8_P, UPHY_RX8_N, UPHY_RX9_P, UPHY_RX9_N, UPHY_RX10_P, UPHY_RX10_N, UPHY_RX11_P, UPHY_RX11_N, UPHY_RX12_P, UPHY_RX12_N, UPHY_RX13_P, UPHY_RX13_N, UPHY_RX14_P, UPHY_RX14_N, UPHY_RX15_P, UPHY_RX15_N, UPHY_RX16_P, UPHY_RX16_N
- UPHY2:** UPHY_TX0_P, UPHY_TX0_N, UPHY_TX1_P, UPHY_TX1_N, UPHY_TX2_P, UPHY_TX2_N, UPHY_TX3_P, UPHY_TX3_N, UPHY_TX4_P, UPHY_TX4_N, UPHY_TX5_P, UPHY_TX5_N, UPHY_TX6_P, UPHY_TX6_N, UPHY_TX7_P, UPHY_TX7_N
- UPHY3:** UPHY_TX8_P, UPHY_TX8_N, UPHY_TX9_P, UPHY_TX9_N, UPHY_TX10_P, UPHY_TX10_N, UPHY_TX11_P, UPHY_TX11_N, UPHY_TX12_P, UPHY_TX12_N, UPHY_TX13_P, UPHY_TX13_N, UPHY_TX14_P, UPHY_TX14_N, UPHY_TX15_P, UPHY_TX15_N, UPHY_TX16_P, UPHY_TX16_N

[illegible]

Reference clocks

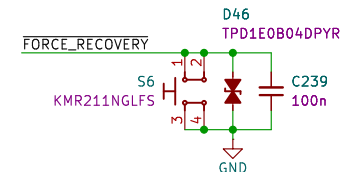
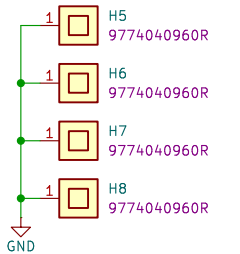
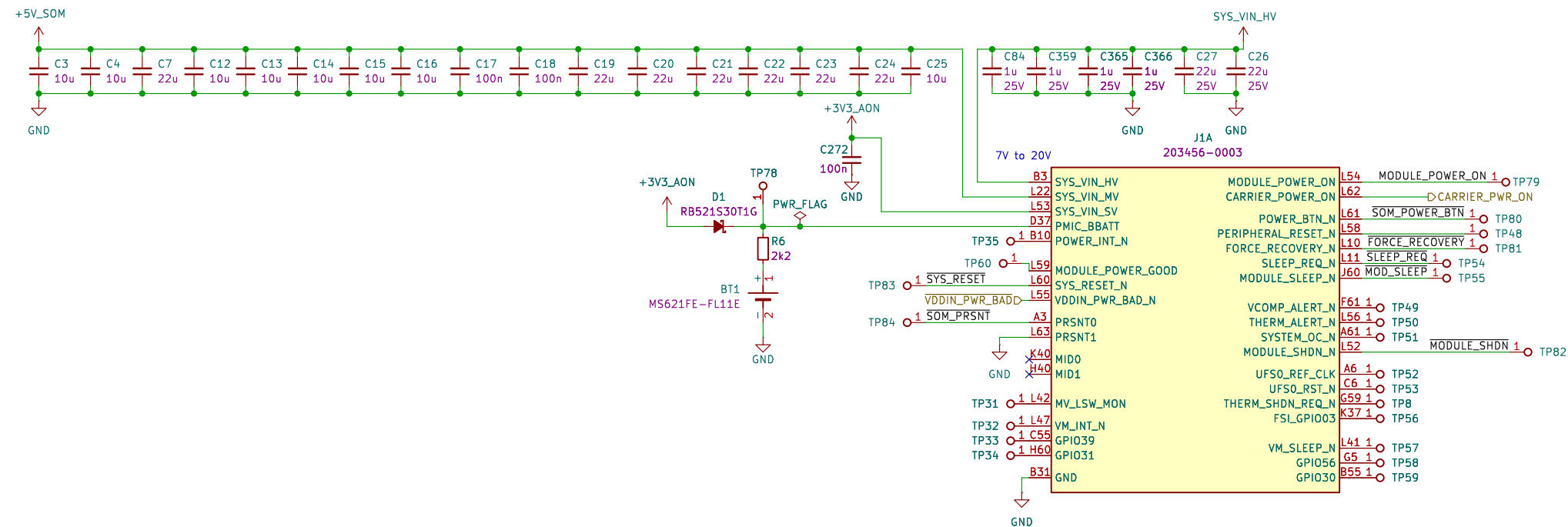
The image shows two circuit diagrams for reference clocks, labeled Y5 and Y1.

Y5 (AK31PHEF1-156.2500T): This is a 156.25MHz clock source. It is connected to a +3V3 supply via a 100nF capacitor (C199) and a 100k resistor (R1). The clock signal is differential, with pins 4 and 5 labeled SFI_CLK+ and SFI_CLK-. The output is connected to SFI_REFCLK+ and SFI_REFCLK- via 33R resistors (R2, R3) and 49R9 resistors (R4, R5).

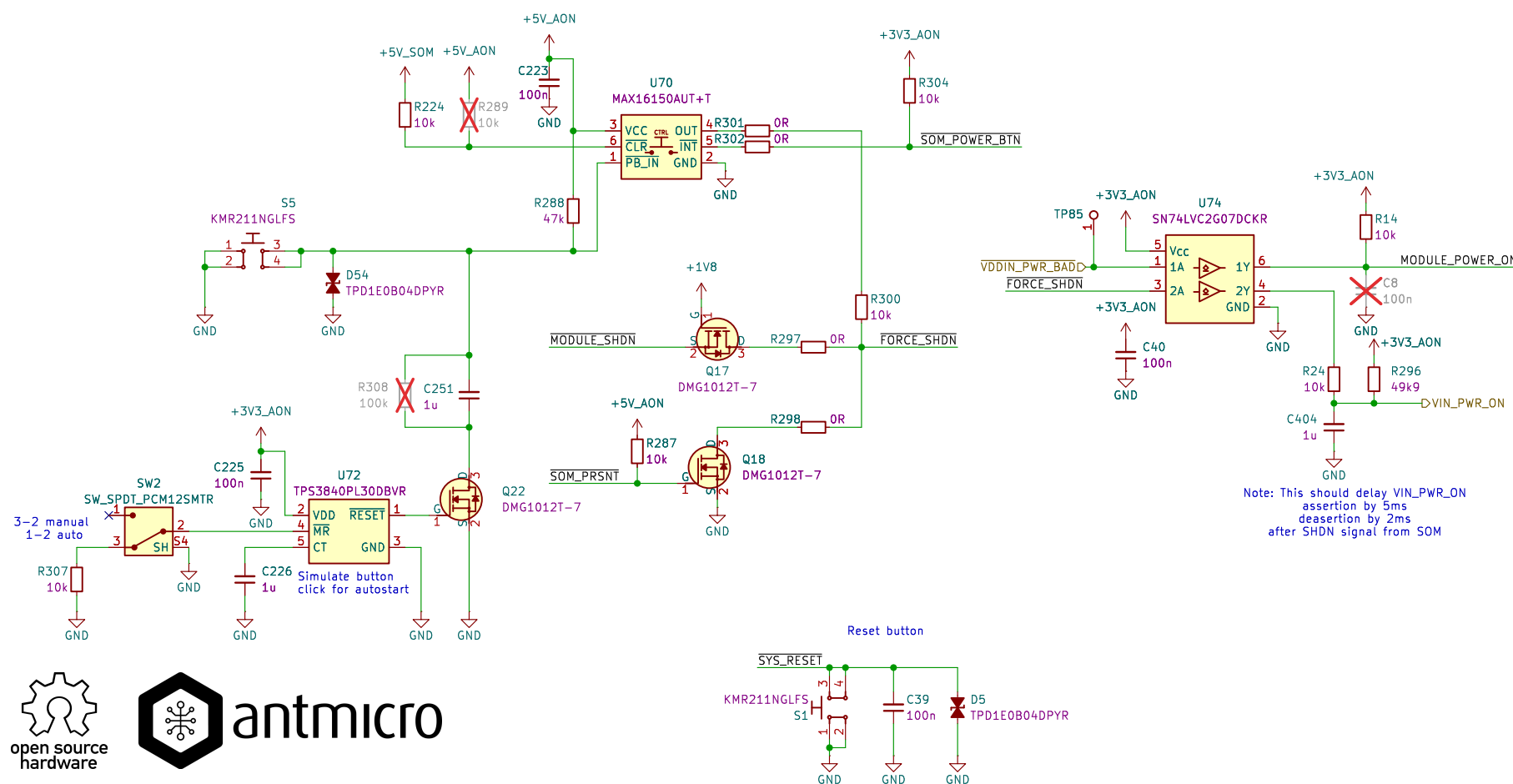
Y1 (NX3241E0100.000000): This is a 100 MHz clock source. It is connected to a +3V3 supply via a 100nF capacitor (C11) and a 100k resistor (R11). The clock signal is differential, with pins 4 and 5 labeled C2_CLK+ and C2_CLK-. The output is connected to C2_REFCLK+ and C2_REFCLK- via 33R resistors (R8, R9) and 49R9 resistors (R191, R193).

CAM0.CSI3_D1-	G45	CSI3_D1_P	CSI7_D1_P	C47	CSI7_D1_N	C48	CAM3.CSI7_D1-										
J1G																	
203456-0003																	
X F40	FSL_GPI000	FSL_GPI020	B9														
X D40	FSL_GPI001	FSL_GPI021	J10														
X B40	FSL_GPI002	FSL_GPI022	K9														
X K36	FSL_GPI004	FSL_GPI023	E31														
X J38	FSL_GPI005	FSL_GPI024	E30														
X J39	FSL_GPI006	FSL_GPI025	D9														
X D36	FSL_GPI011	FSL_GPI026	B5														
X B48	FSL_GPI016	FSL_GPI027	K7														
X B49	FSL_GPI017																
www.antmicro.com																	
Antmicro Ltd																	
Sheet: /SoM_I02/																	
File: som_io2.kicad_sch																	
Title: Jetson AGX Thor Baseboard																	
Size: A3		Date: 2025-11-03				Rev: 1.1.0:199dd00f											
KiCad E.D.A. 9.0.6						Id: 3/15											

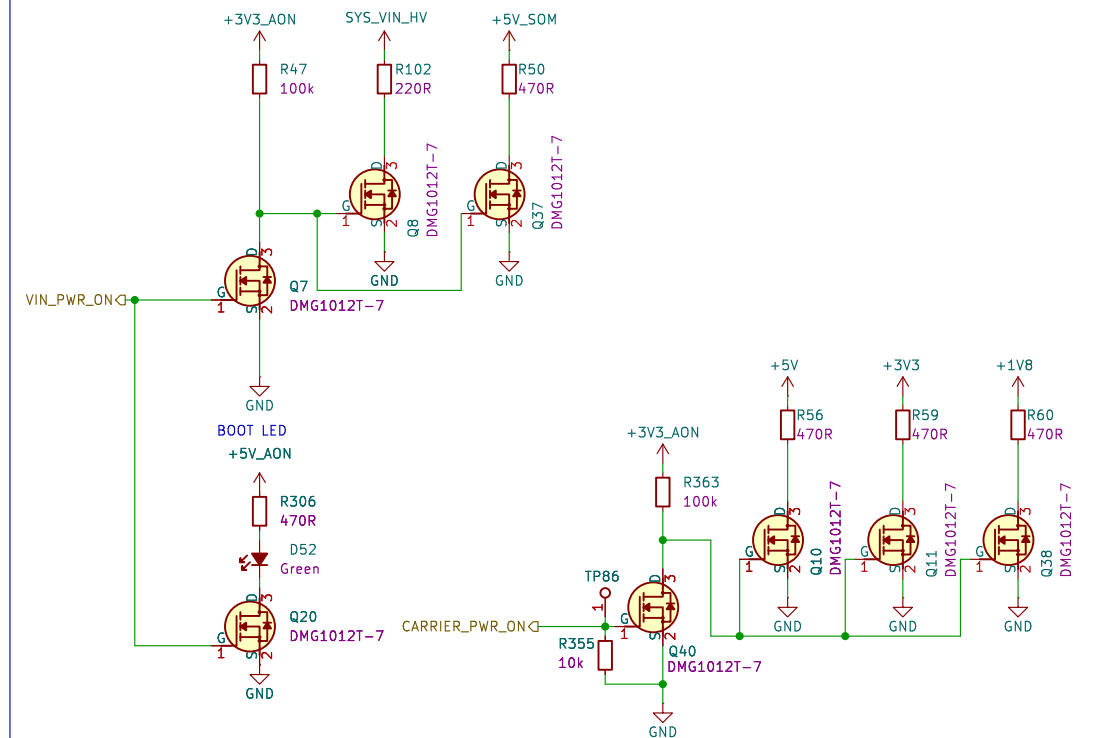
SoM Power



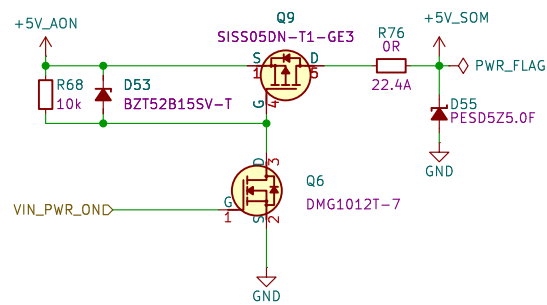
Power-up and reset



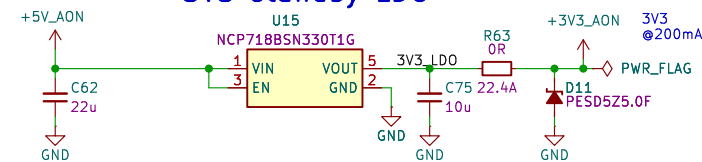
Discharge circuit



SoM Medium voltage power switch

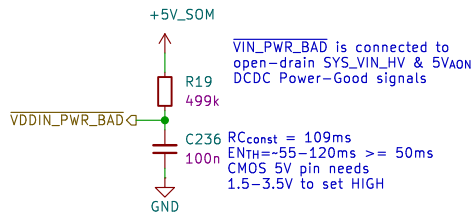


3V3 standby LDO

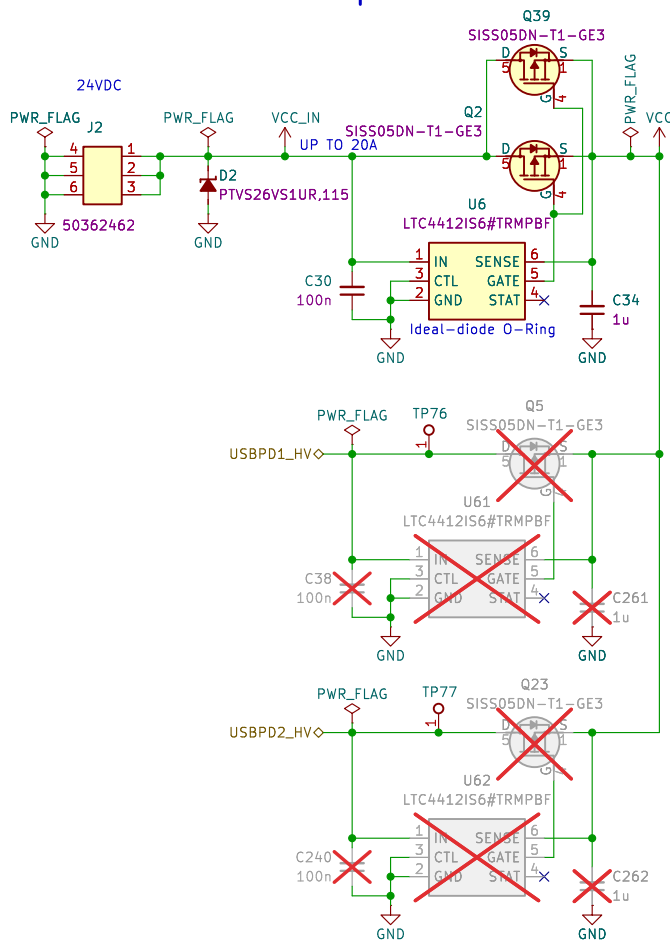


Power sequencing

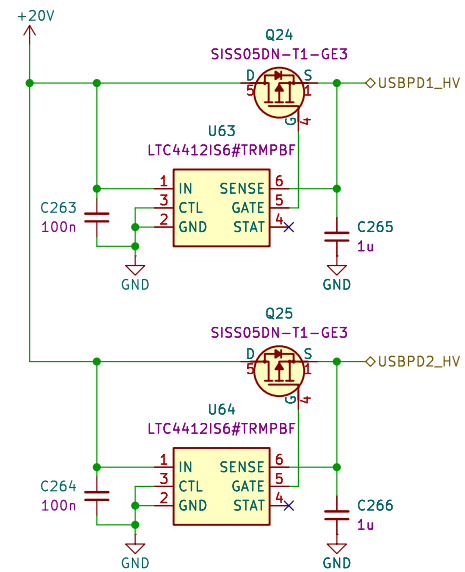
Sequence	Power rail	EN_signal	Delay
1	VCC(24V)	-	0
2	+5V_AON	VCC pull-up	0
3	+3V3_AON	5V_AON	0
4	+5V_SOM	VIN_PWR_ON	>=20ms
	SYS_VIN_HV	VIN_PWR_ON	>=20ms
5	MODULE_POWER_ON	+5V_SOM & PG(SYS_VIN_HV)	>=50ms
6	+3V3	CARIER_POWER_ON	
	+1V8	CARIER_POWER_ON	
	+12V	CARIER_POWER_ON	
	+5V	CARIER_POWER_ON	



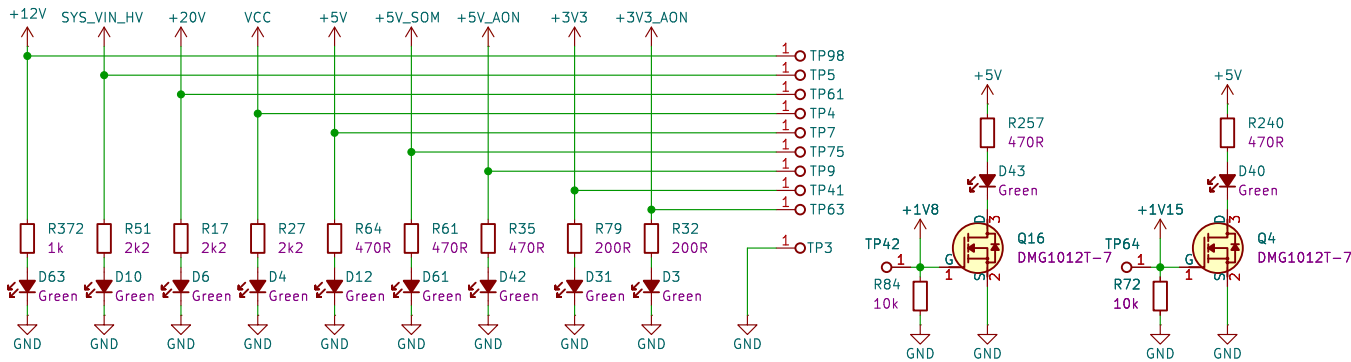
Input selector



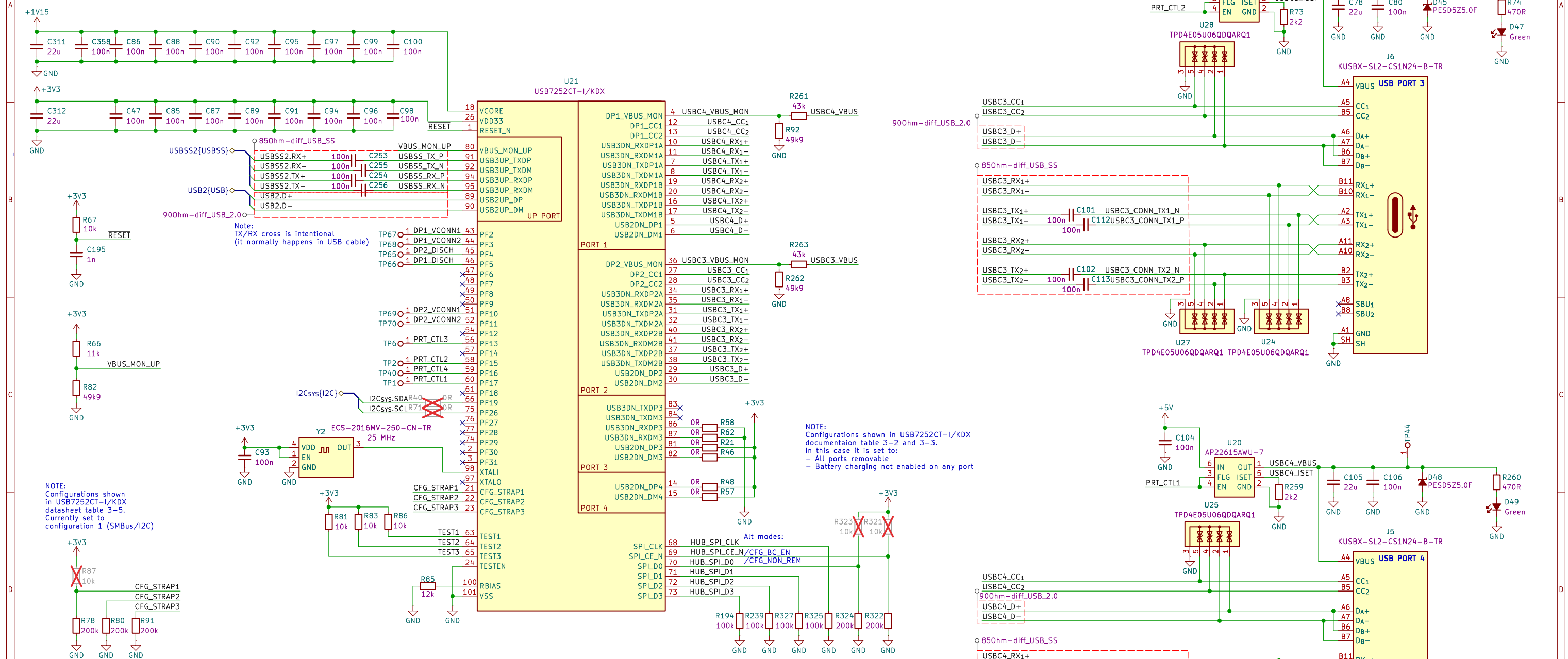
USB PD Power Ideal Diodes



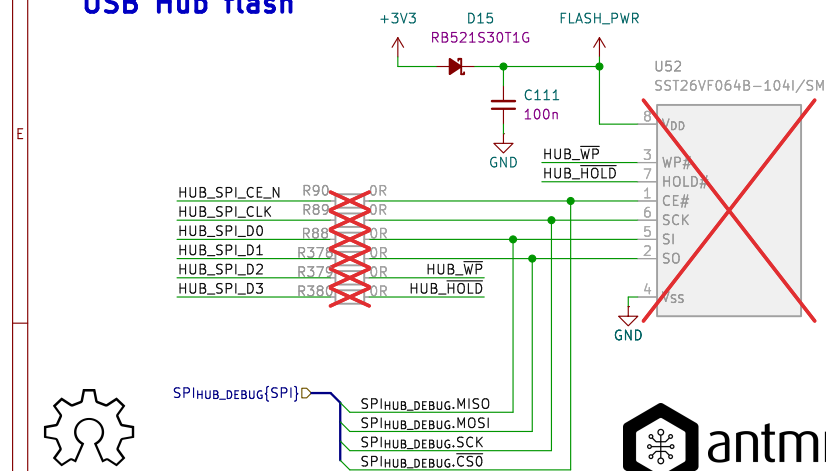
Power LEDs and testpoints



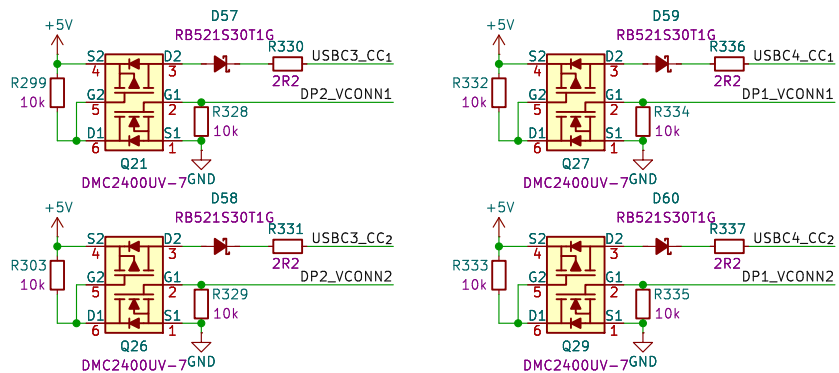
USB hub



USB Hub flash

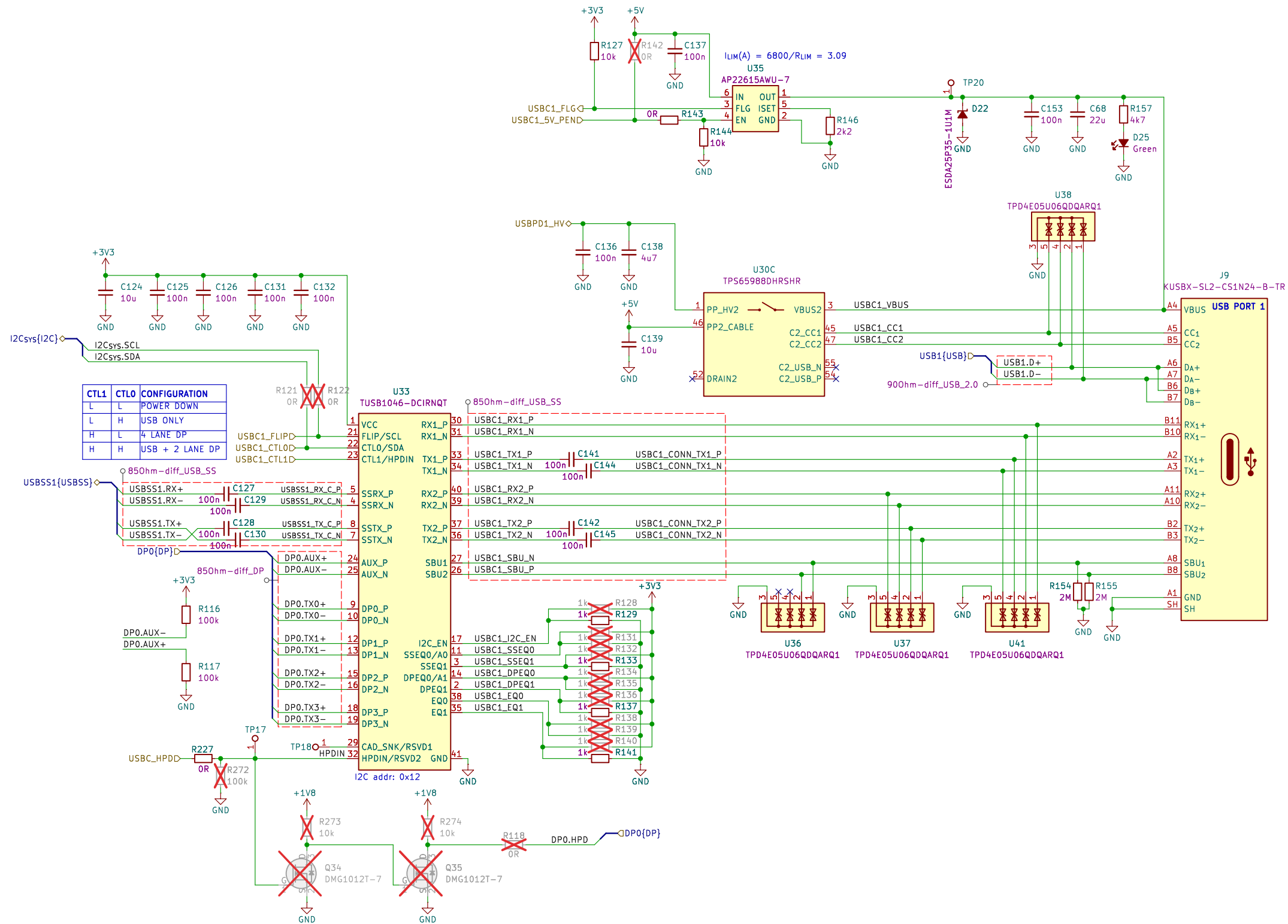


VCONN Switches

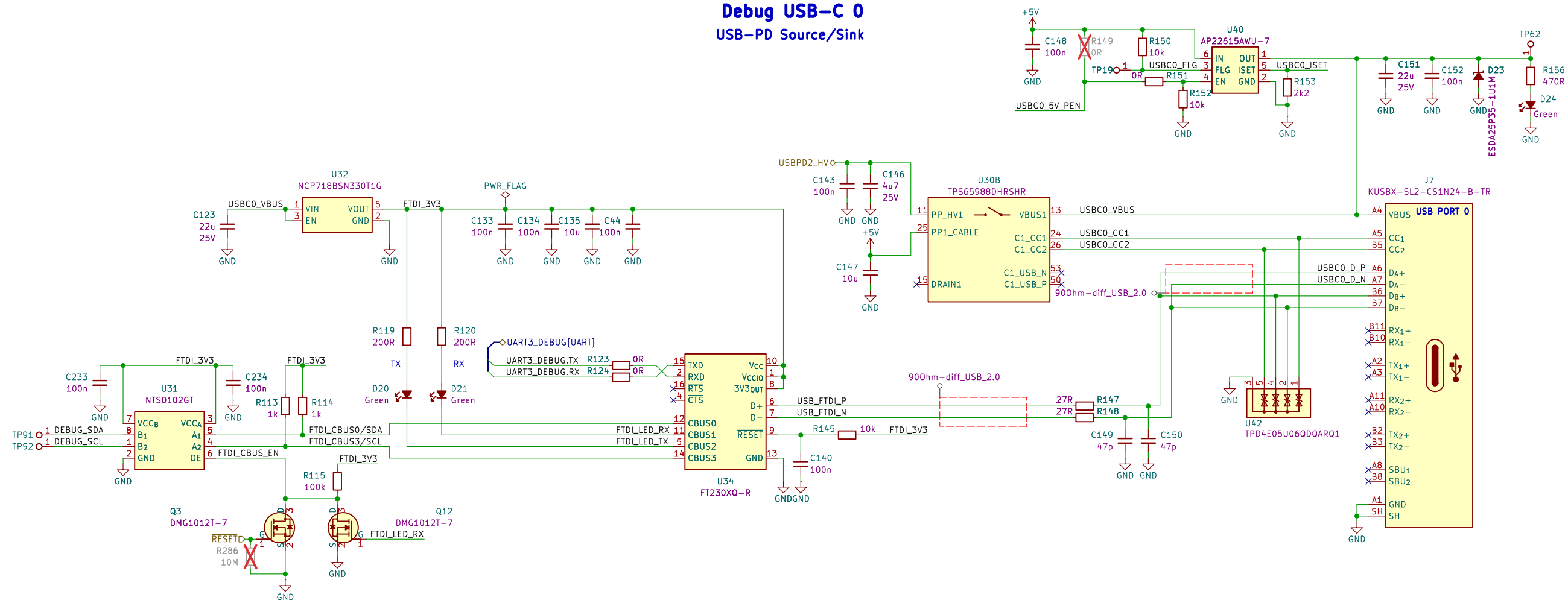


[illegible]

USB Display port alt mode

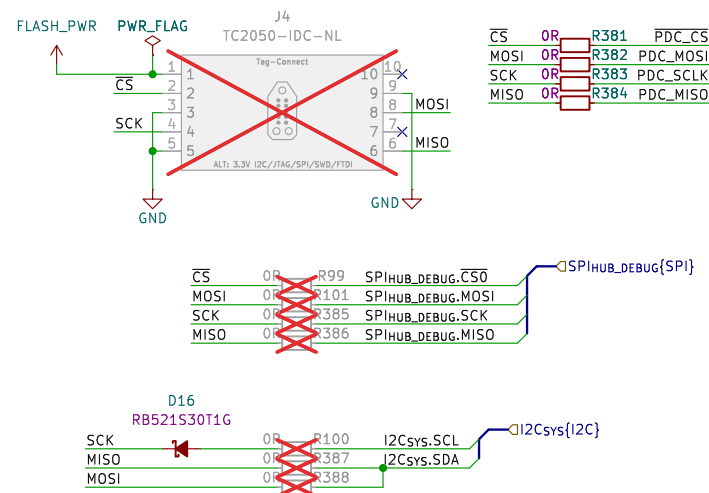


Debug USB-C 0

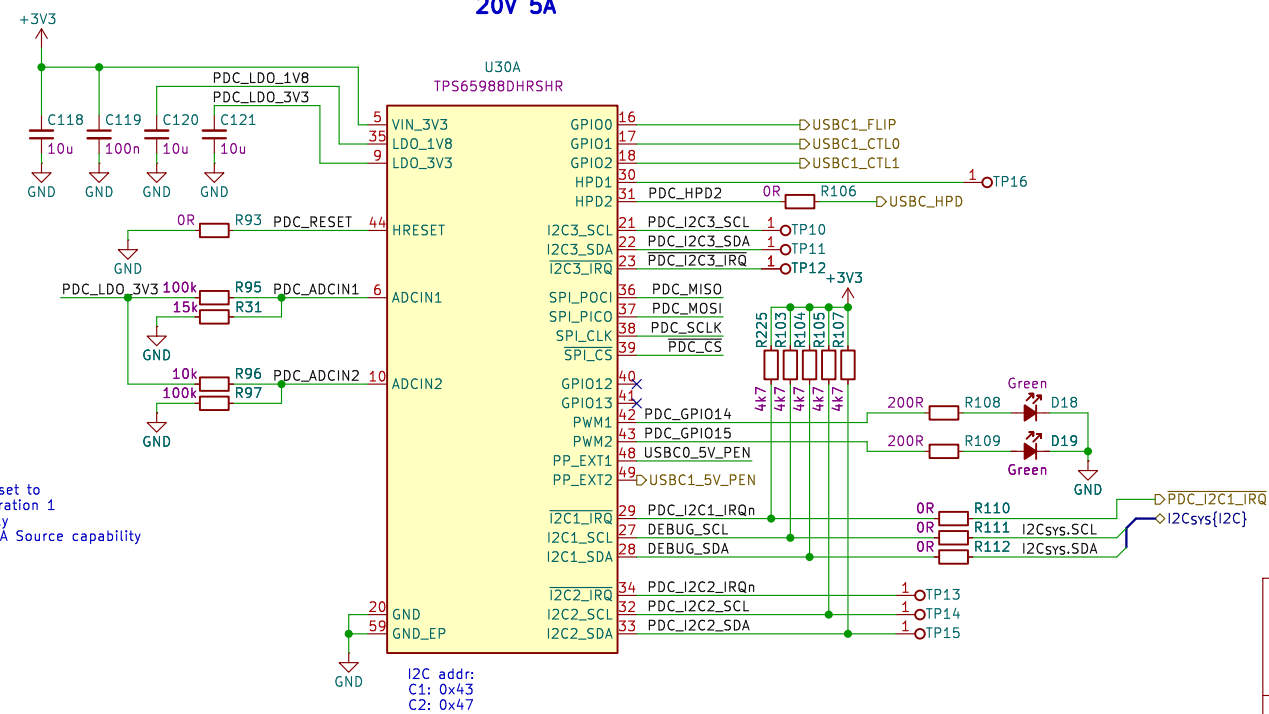


Debug connector

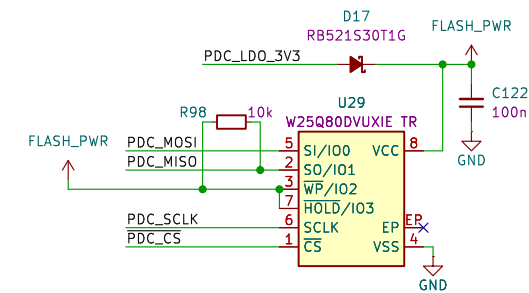
pinout compatible with
www.github.com/antmicro/ftdi-toolkit



USB PD controller
20V 5A



NOTE:
Device set to
configuration 1
DFP only
5V at 3A Source capability



www.antmicro.com

Antmicro Ltd

Sheet: /USB Debug, PD/
File: usb_debug_pd.kicad_

Title: Jetson AGX Thor Baseboard

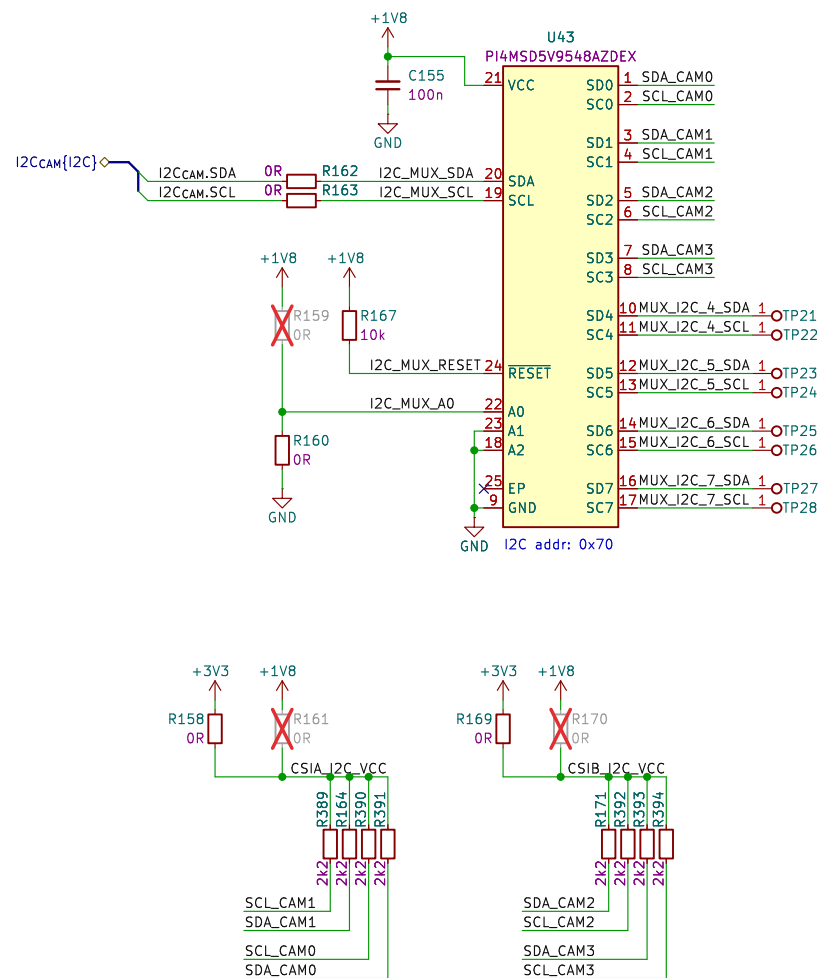
Size: A3

Date: 2025-11-03

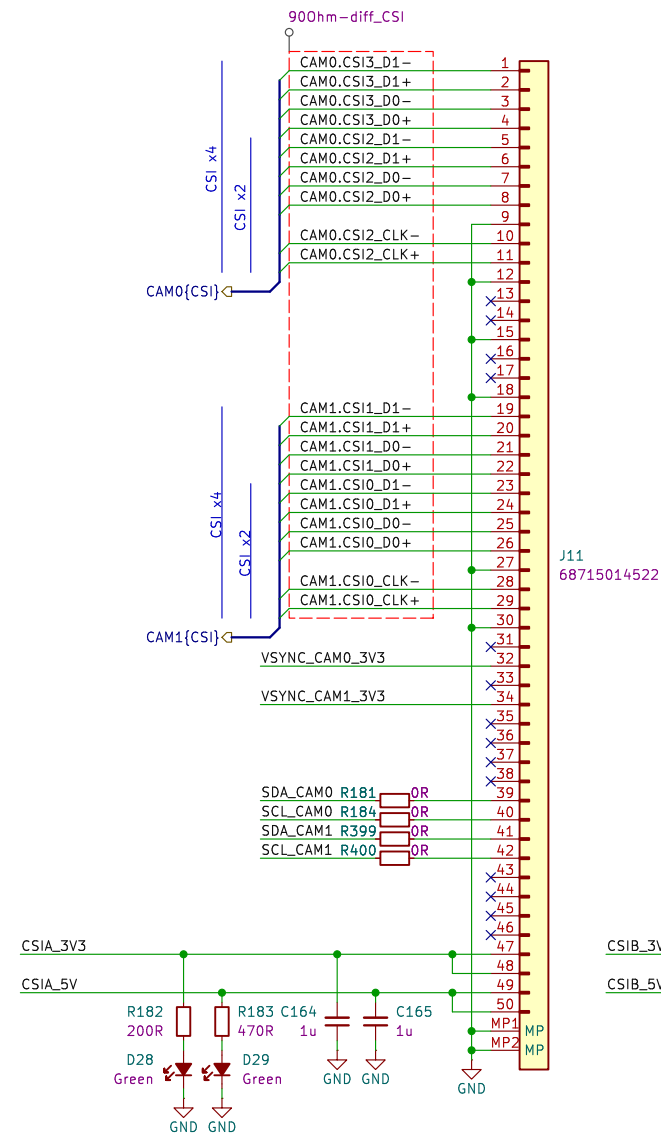
Rev: 1.1.0:199dd00f

Id: 9/15

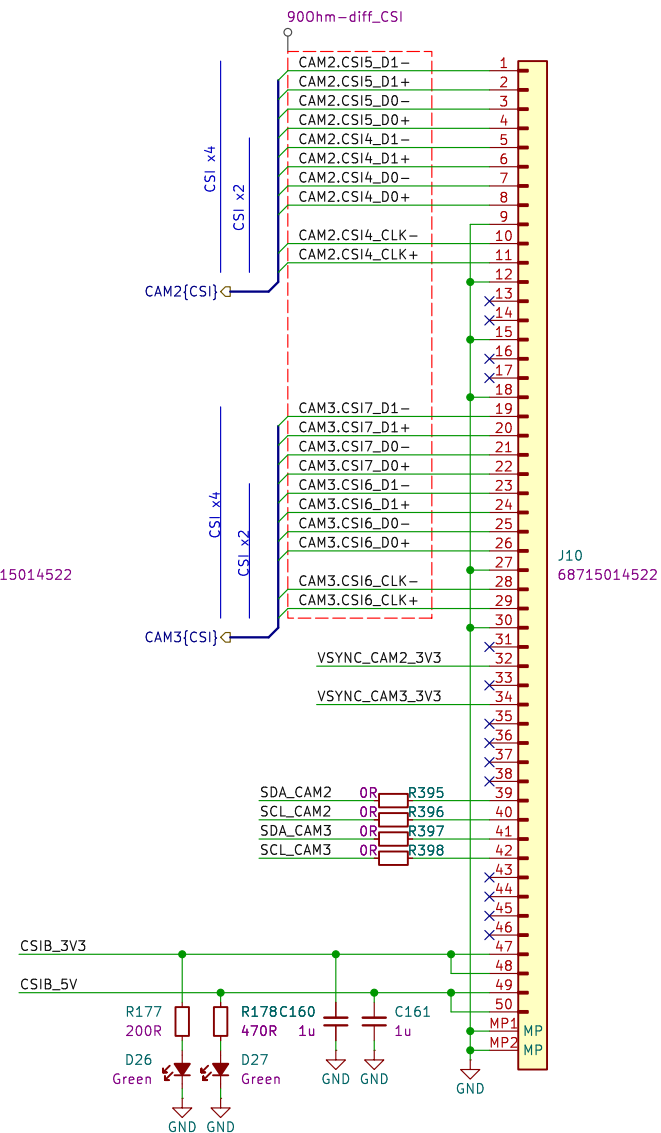
I2C Mux



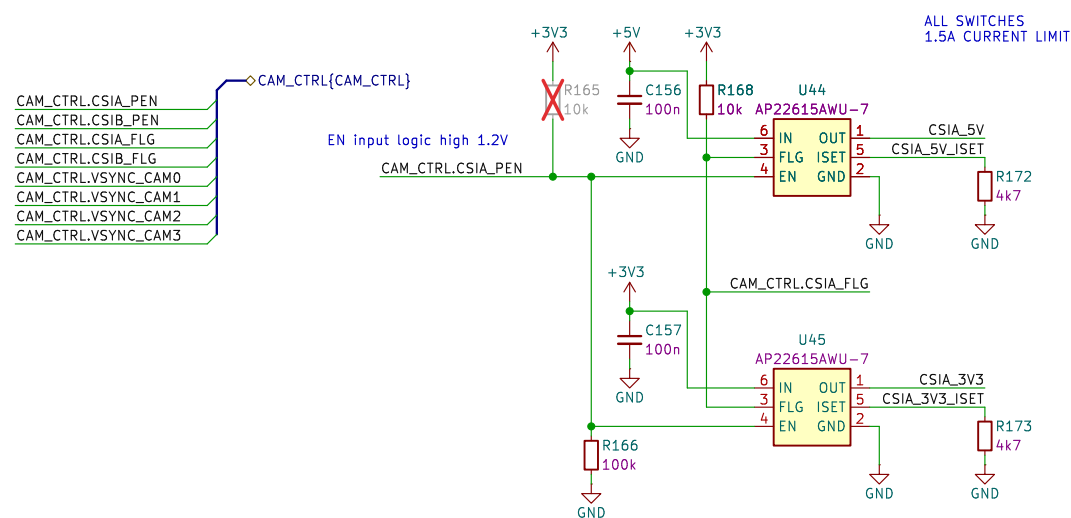
CSI Connector A



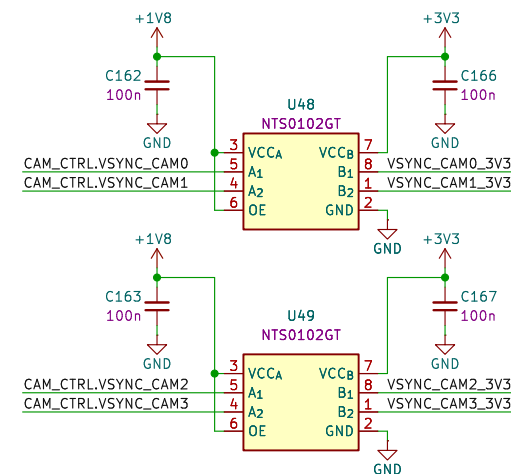
CSI Connector B

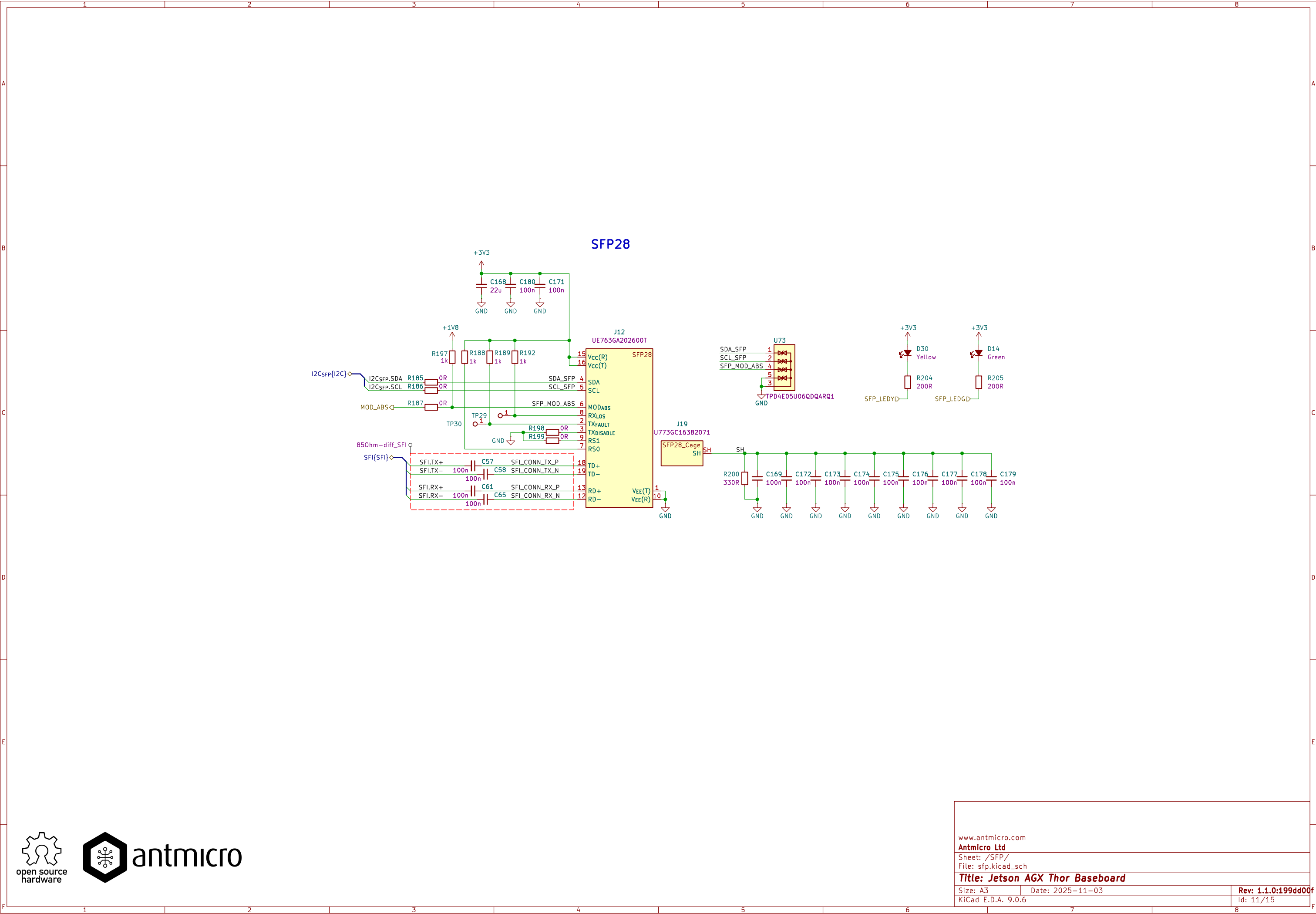


Power switches



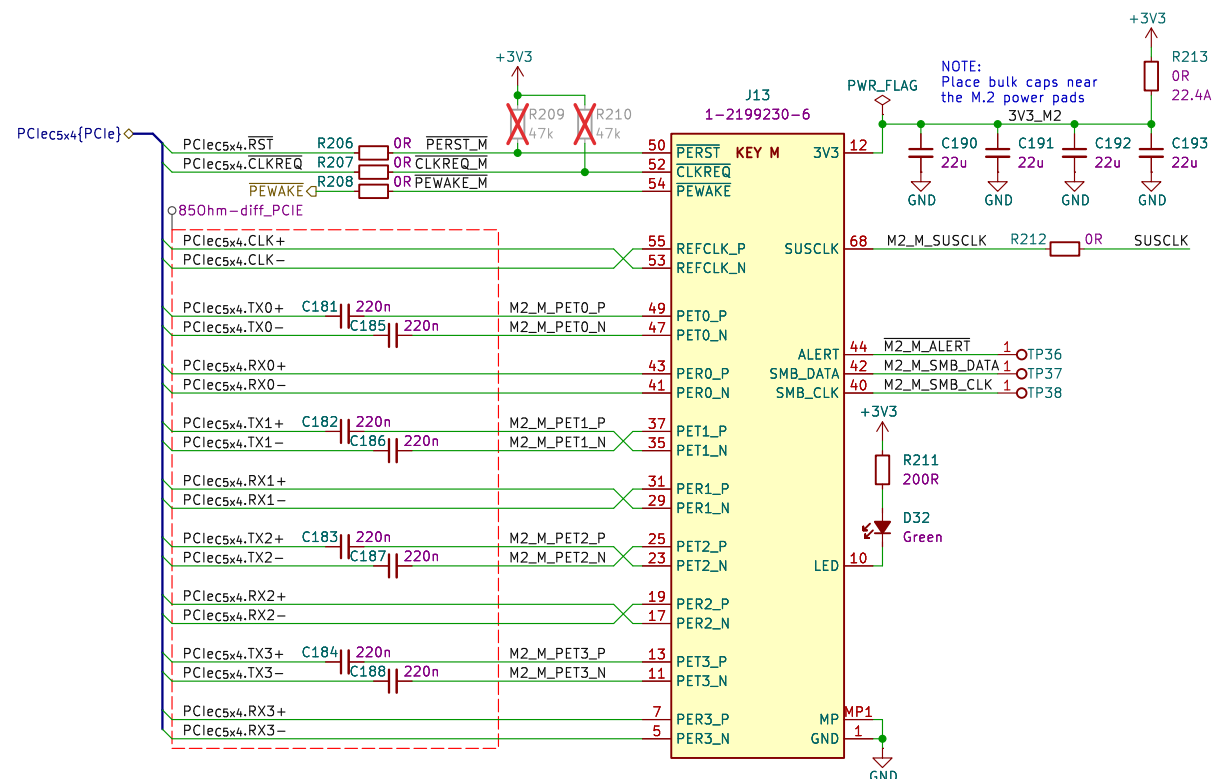
Level shifters





M.2 key M

PCIe x4

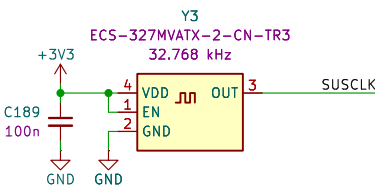


NOTE:
Nvidia Jetson AGX Thor
supports polarity inversion

A1
Mech_M2_2280_H2.5mm

H9
Spacer_Drill3.7mm_H2.5mm_9774025151R

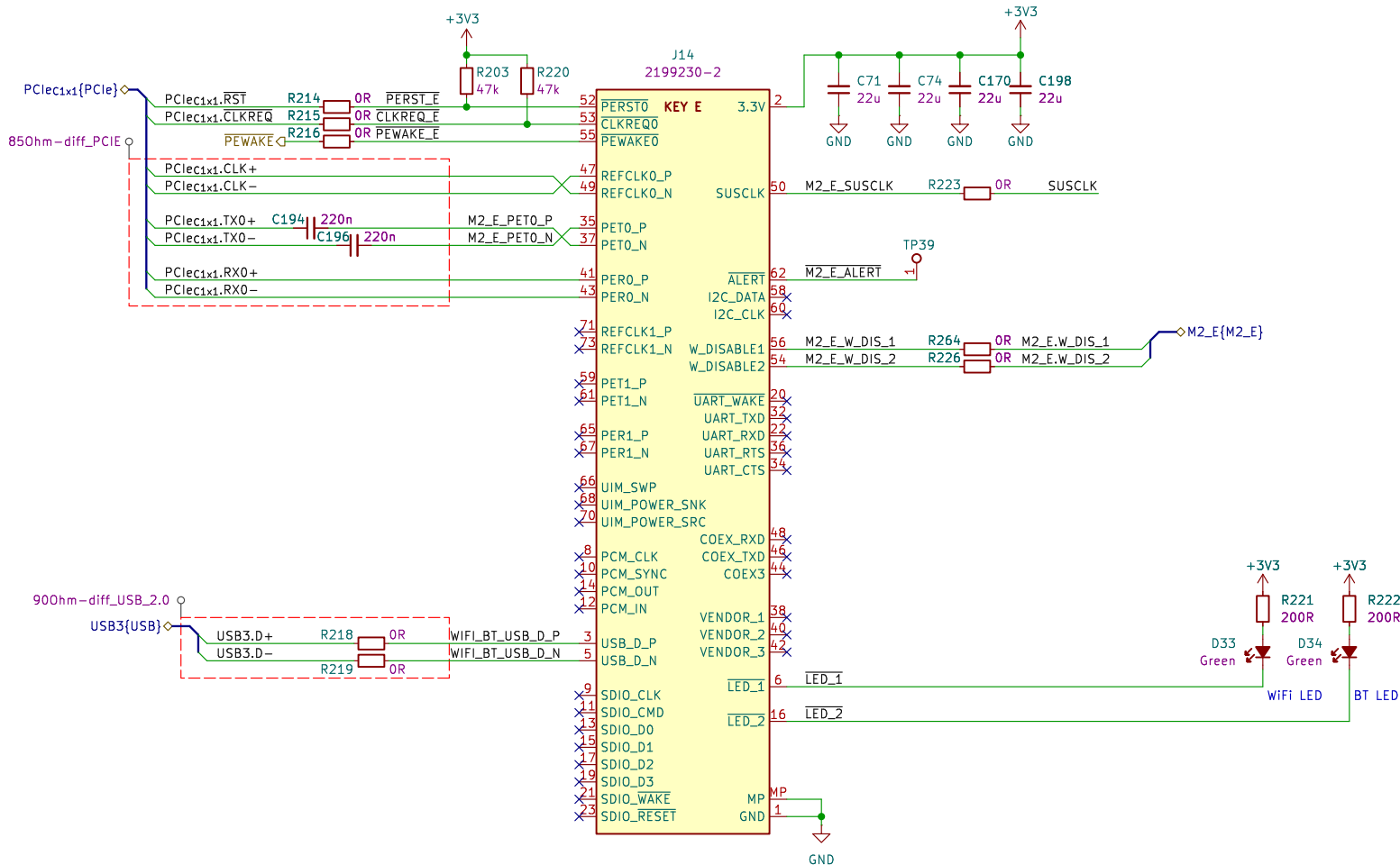
SUSCLK SOURCE



antmicro

M.2 key E

2x PCIe x1, USB 2.0, I2C, UART and PCM



A2
Mech_M2_2242_H2.5mm

H10
Spacer_Drill3.7mm_H2.5mm_9774025151R

www.antmicro.com

Antmicro Ltd

Sheet: /M.2/

File: m2.kicad_sch

Title: Jetson AGX Thor Baseboard

Size: A3

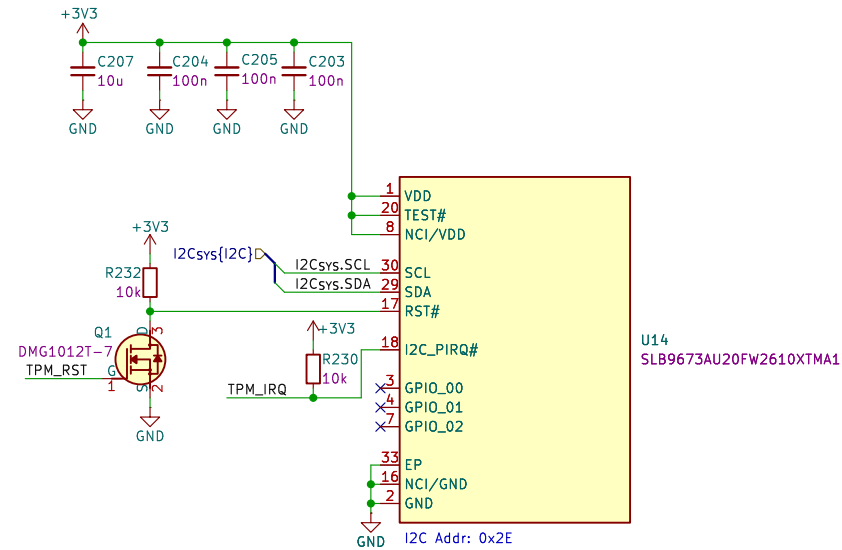
Date: 2025-11-03

Rev: 1.1.0:199dd00f

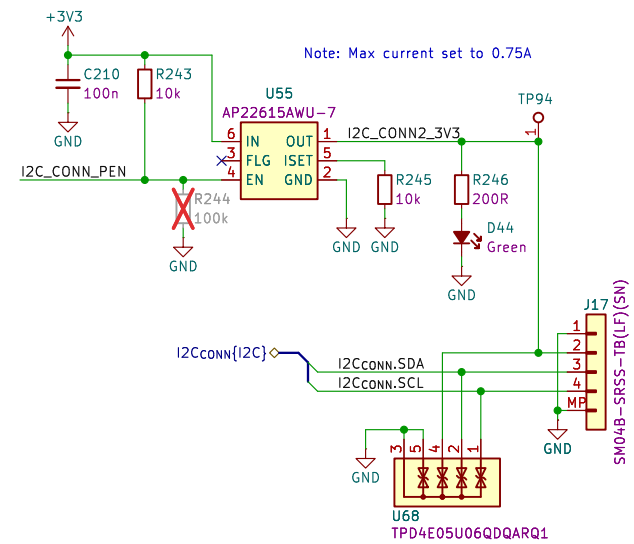
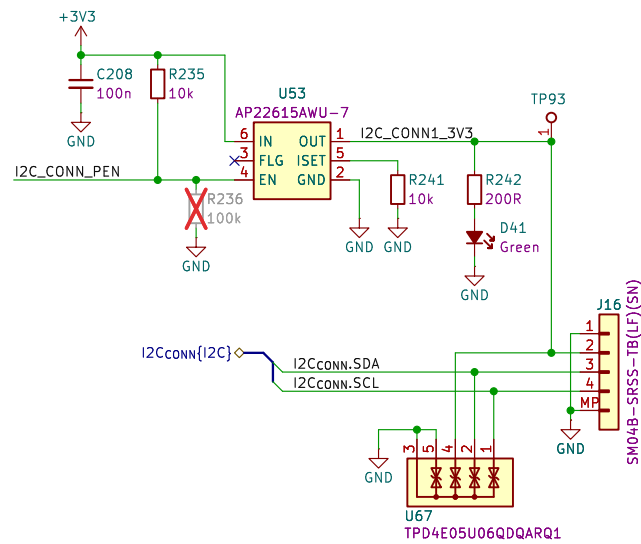
KiCad E.D.A. 9.0.6

Id: 12/15

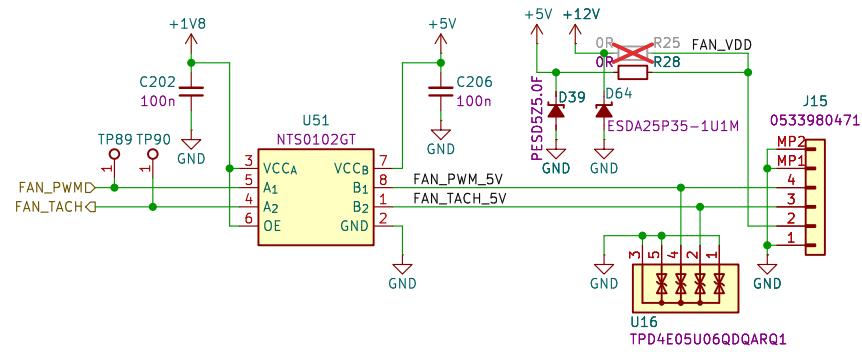
TPM



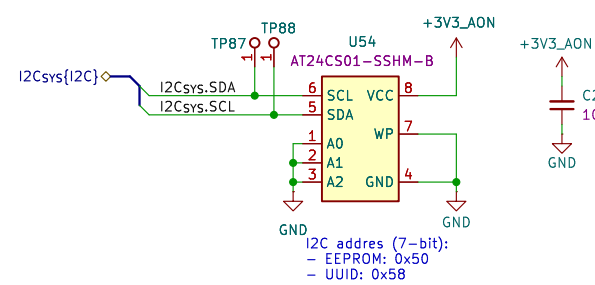
I2C connectors



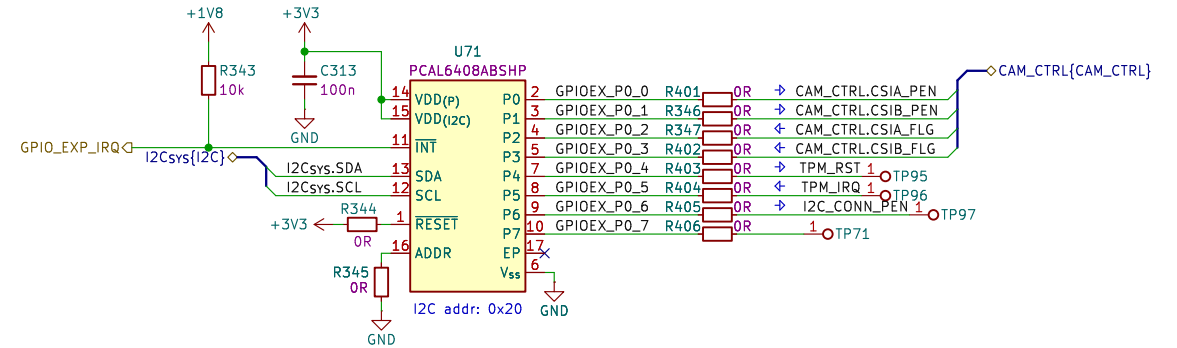
Fan connector



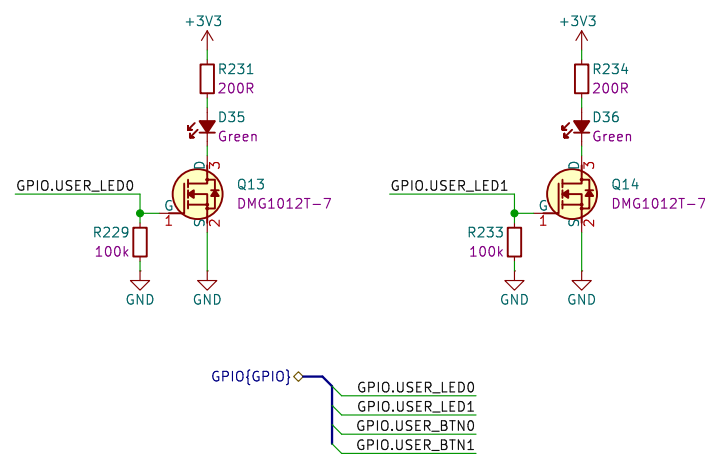
ID EEPROM



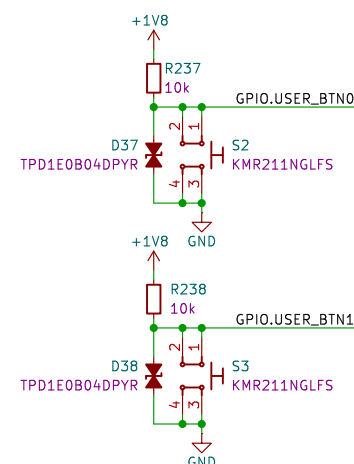
GPIO Expander



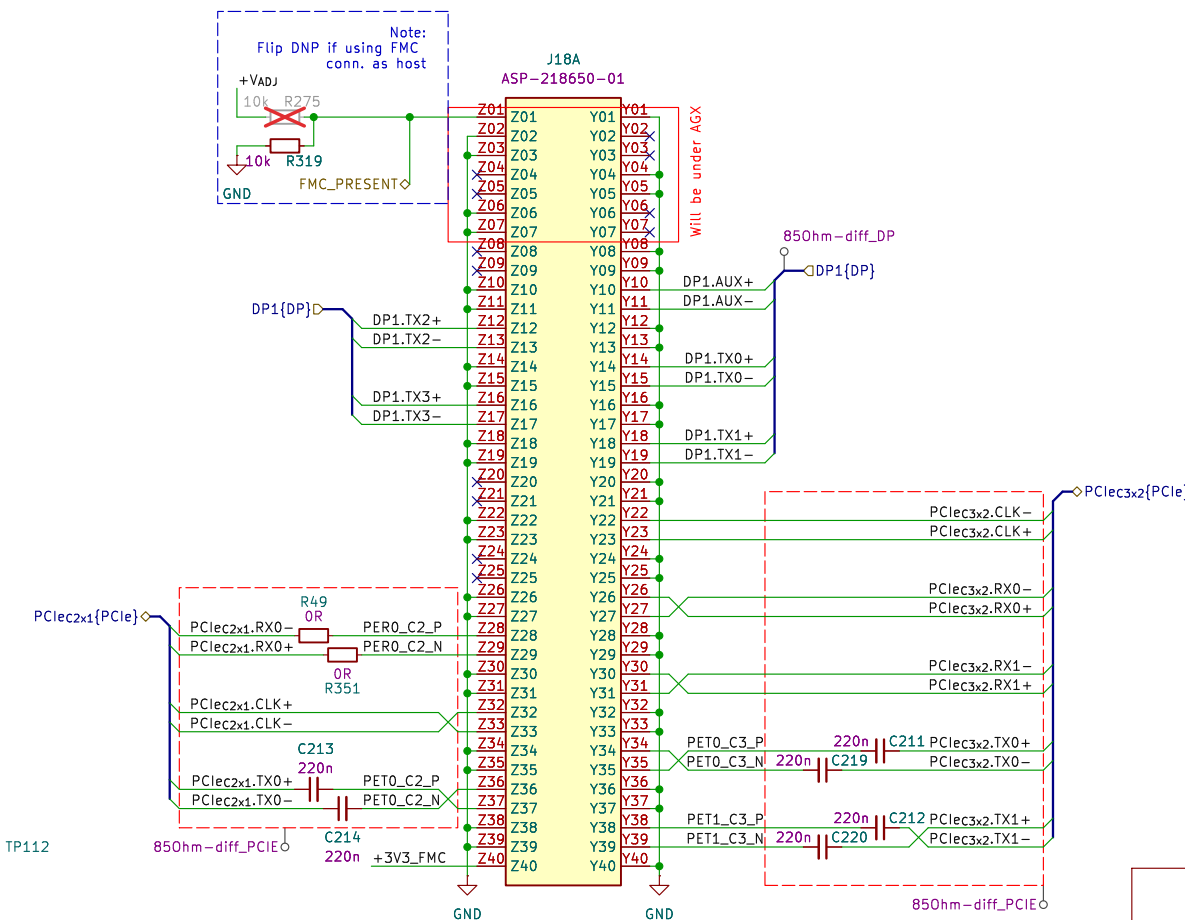
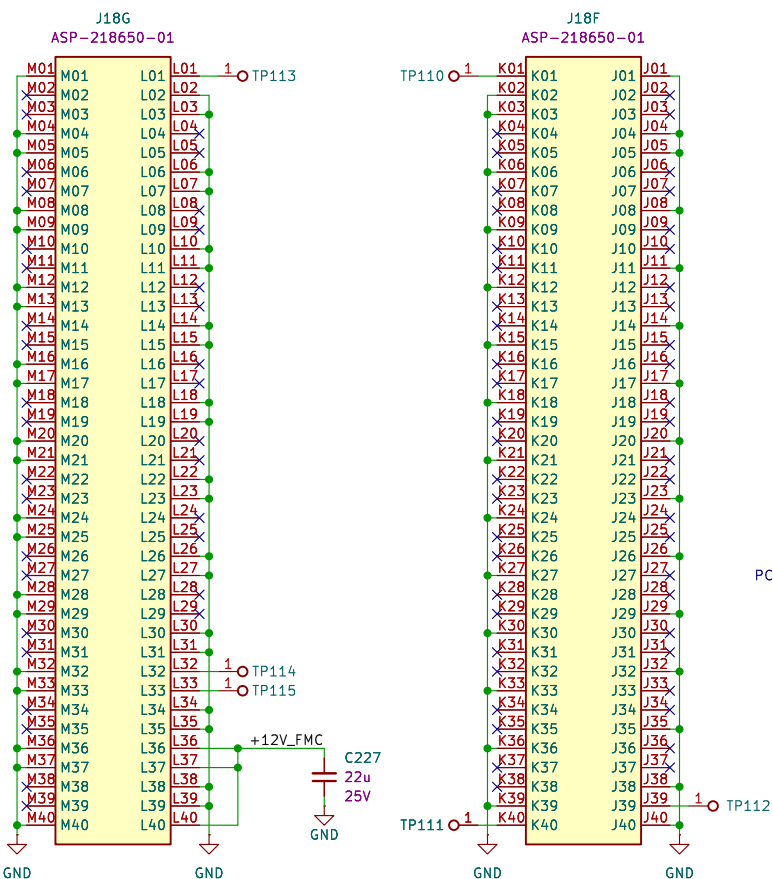
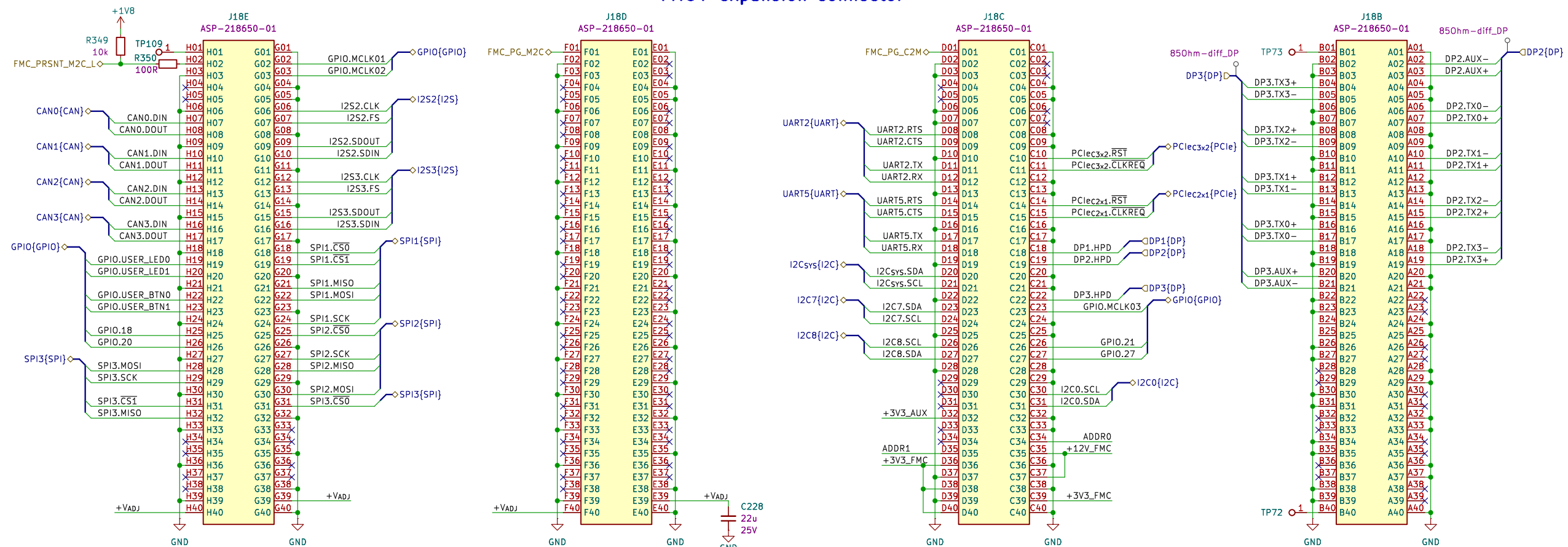
User LEDs



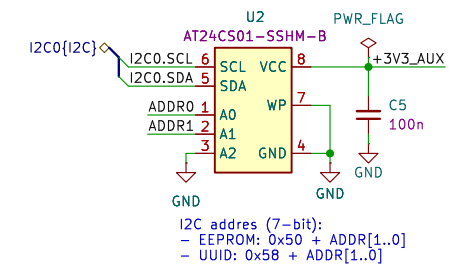
User Buttons



FMC+ expansion connector



FMC Module ID



Power connector

