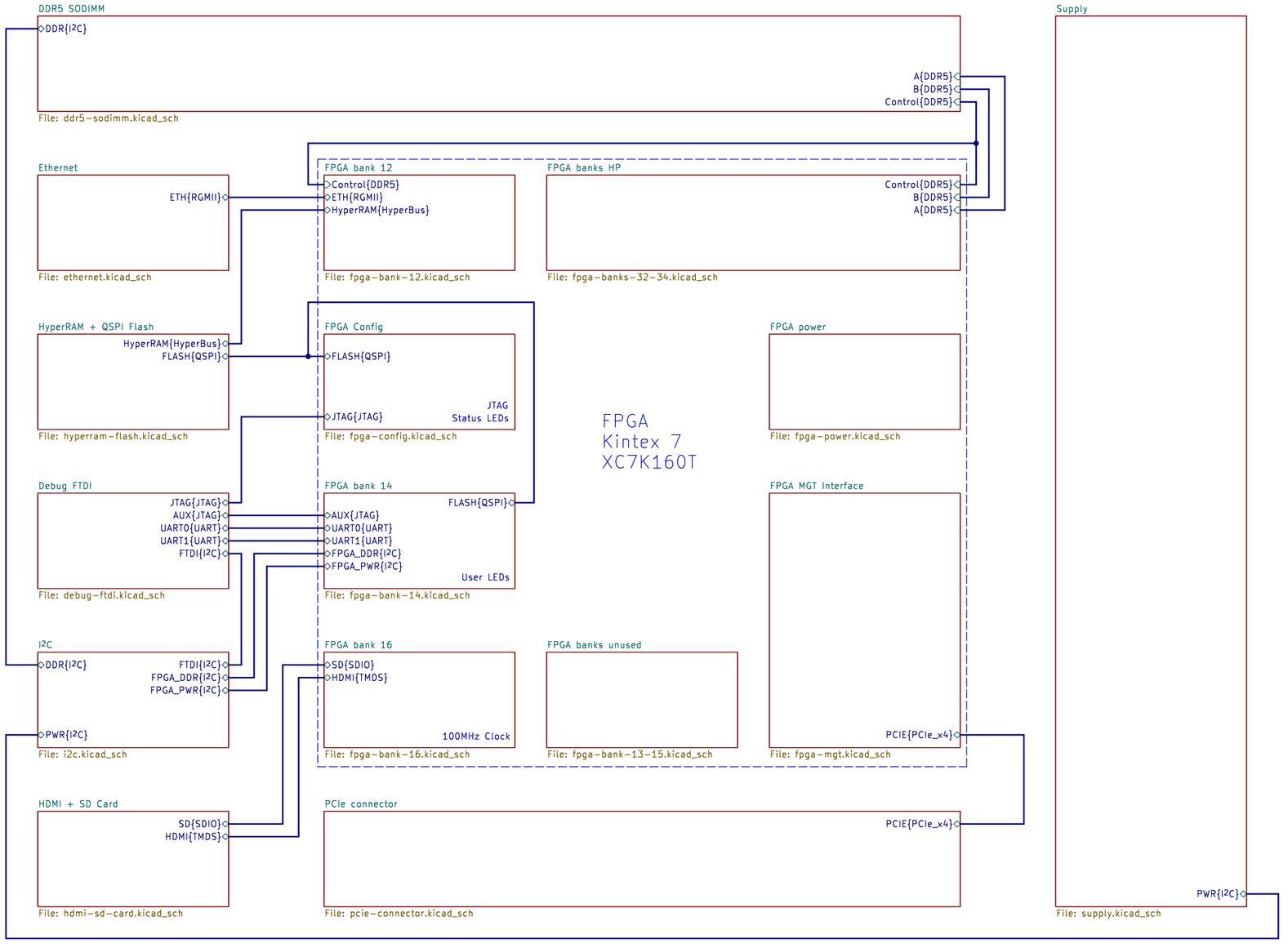
SO-DIMM DDR5 Tester



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Mechanical

H1
960-27-12-D-AB-0

Horizontal lightguide 1x3
H2
Lightpipe_Mentor_1296.2013

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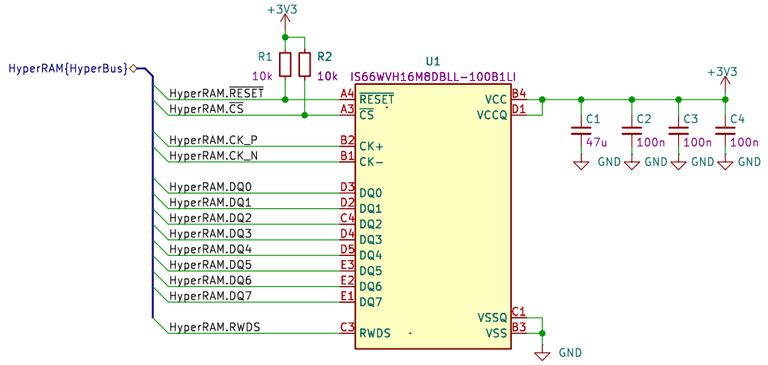
Sheet: /
File: sodimm-ddr5-tester.kicad_sch

Title: SO-DIMM DDR5 Tester

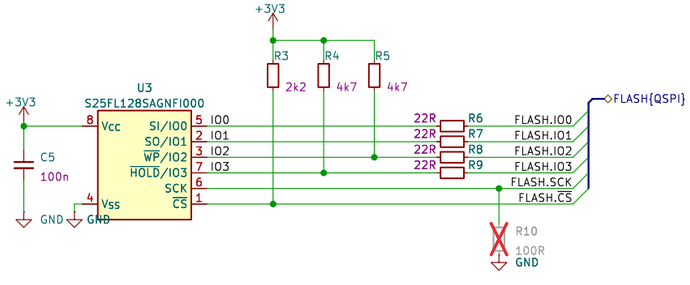
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 1/17

HyperRAM



(Q)SPI flash

Master SPI Quad (x4) configuration scheme
Follows Figure 2–14 7 Series FPGAs Configuration User Guide
UG470 (v1.13.1)



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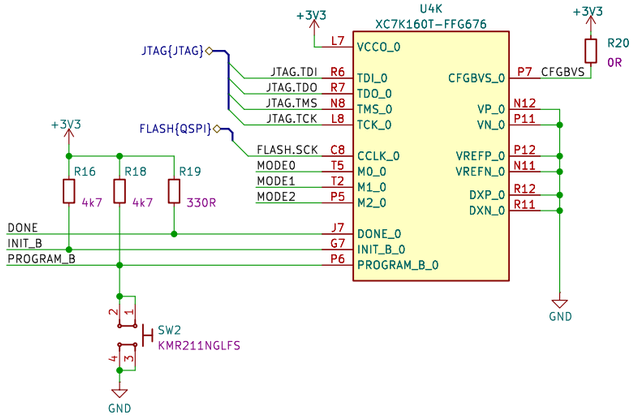
Sheet: /HyperRAM + QSPI Flash/
File: hyperram-flash.kicad_sch

Title: SO-DIMM DDR5 Tester

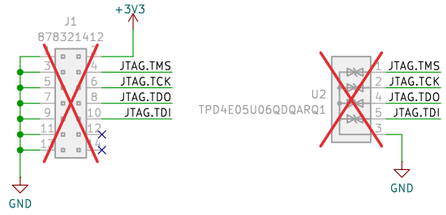
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 2/17

FPGA BANK 0

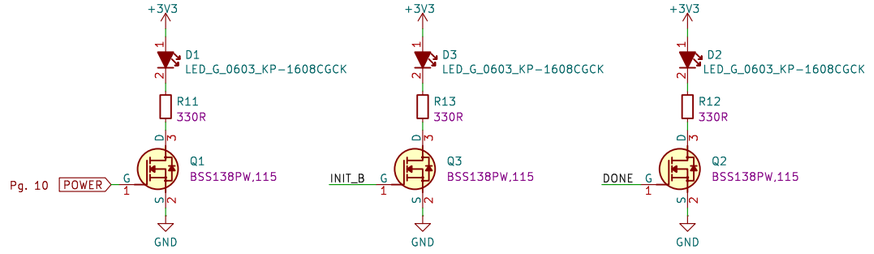


JTAG Connector

Compatible with Xilinx Platform Cable

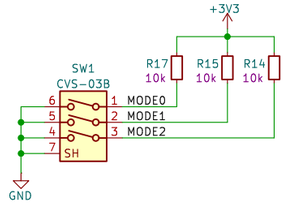


STATUS LEDs



Configuration Modes

For details, see UG470 p. 21



Config. mode	MODE[2:0]
Master Serial	000
Master SPI	001
Master BPI	010
Master SelectMAP	100
JTAG	101
Slave SelectMAP	110
Slave Serial	111

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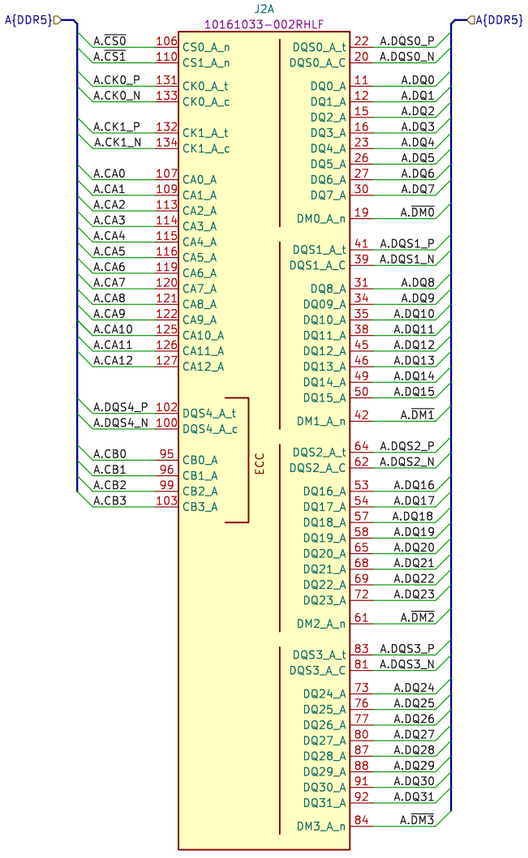
Sheet: /FPGA Config/
File: fpga-config.kicad_sch

Title: SO-DIMM DDR5 Tester

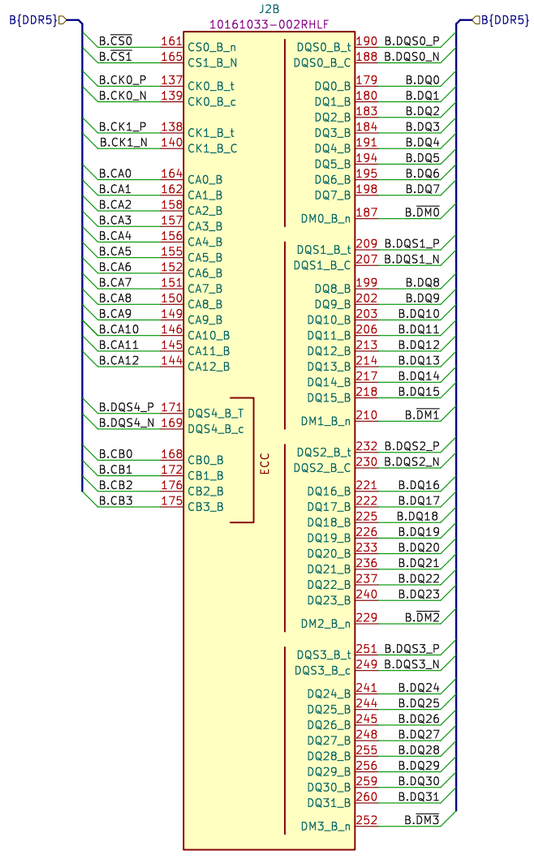
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 3/17

DDR5 SODIMM connector

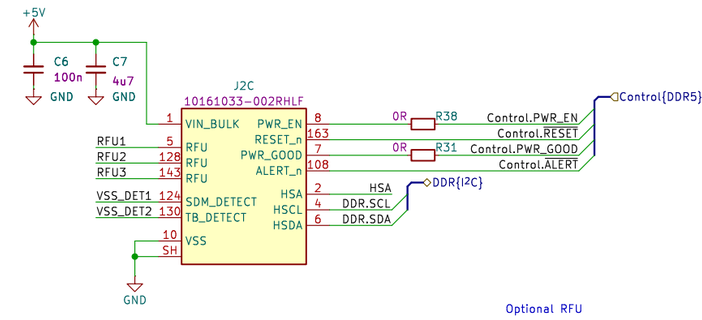
Subchannel A



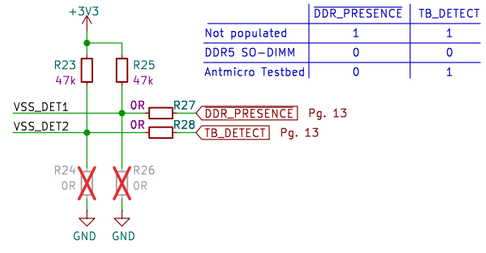
Subchannel B



Power and control

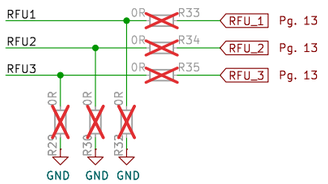


SO-DIMM type detect

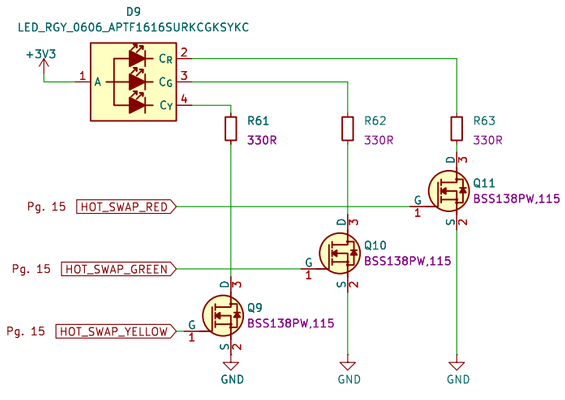


	DDR_PRESENCE	TB_DETECT
Not populated	1	1
DDR5 SO-DIMM	0	0
Antmicro Testbed	0	1

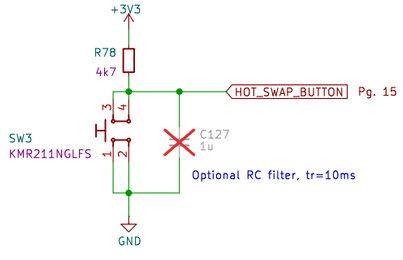
Optional RFU



HOT SWAP status LED

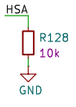


HOT SWAP eject button

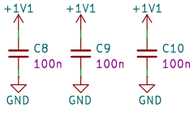


Serial adress select

Default 000



Plane decoupling



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Sheet: /DDR5 SODIMM/
File: ddr5-sodimm.kicad_sch

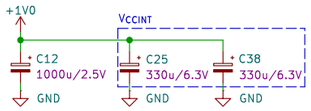
Title: SO-DIMM DDR5 Tester

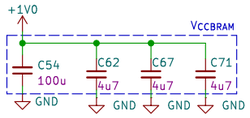
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 4/17

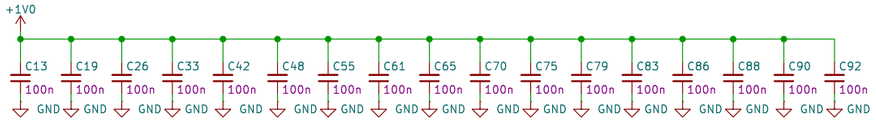
FPGA Power rails

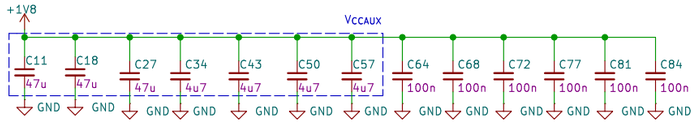
Bank marked by dahed line
referenced from 7 Series FPGAs
PCB Design Guide UG483
(FFG+FBG Package worst case)

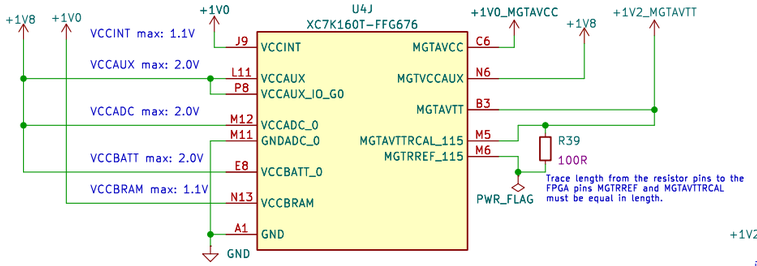
MGT decoupling marked by dahed line
referenced from 7 Series FPGAs
PCB Design Guide UG482
(FFG+FBG Package worst case)

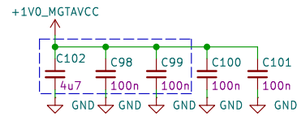


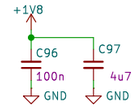


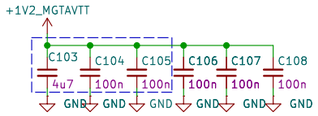


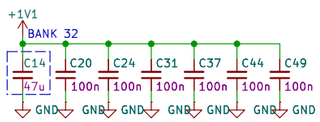


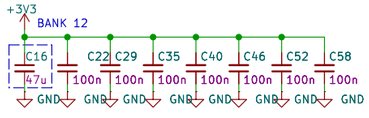


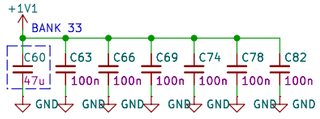


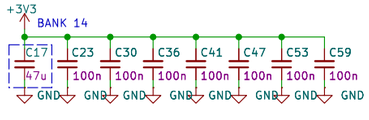


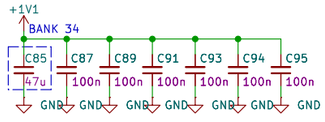


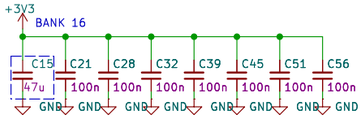












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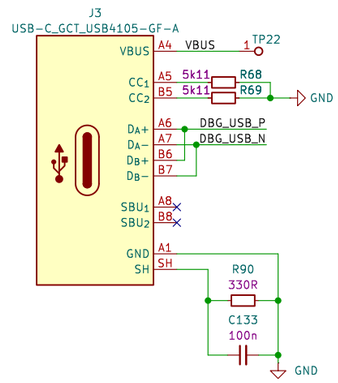
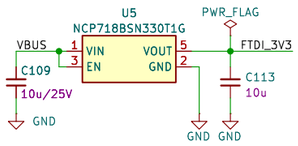
Sheet: /FPGA power/
File: fpga-power.kicad_sch

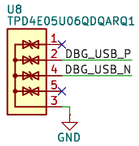
Title: SO-DIMM DDR5 Tester

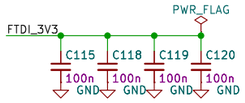
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 5/17

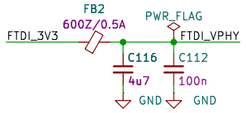
Debug FTDI

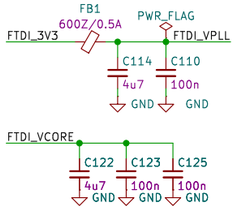


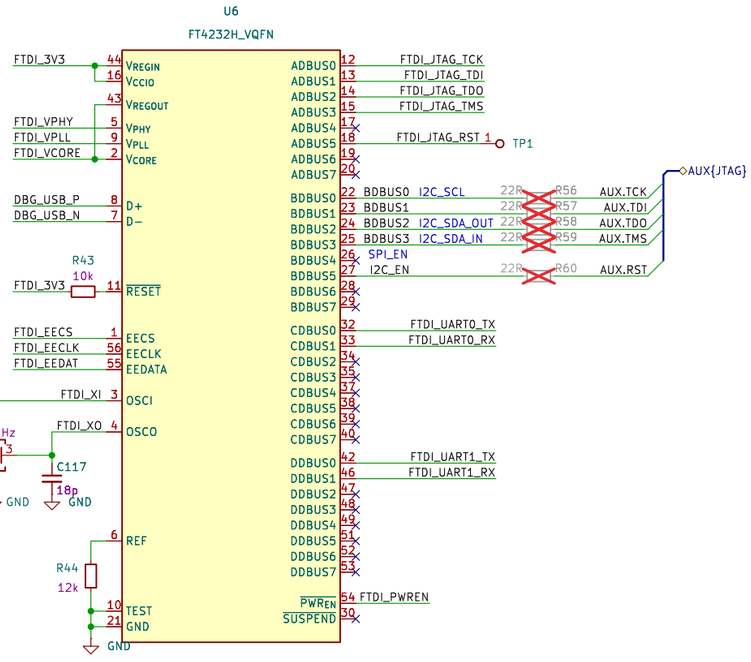


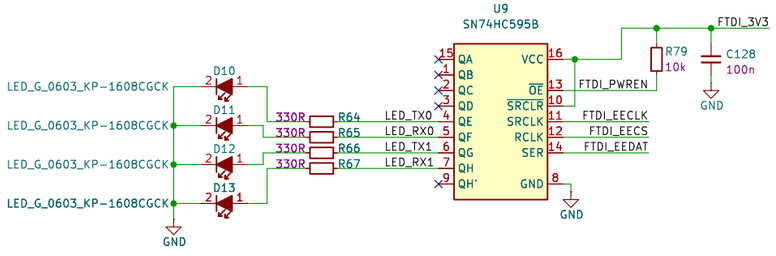


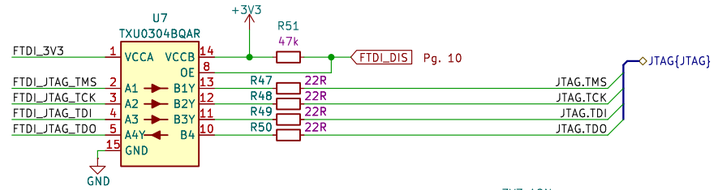


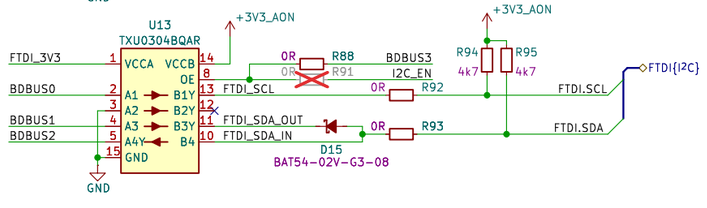


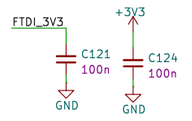


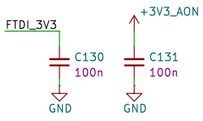


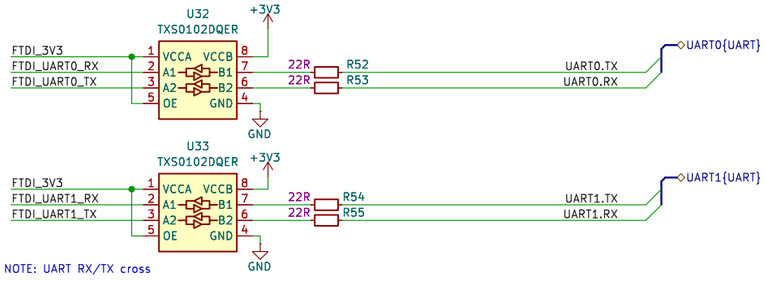


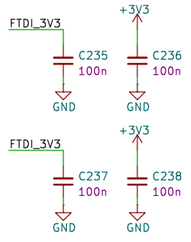






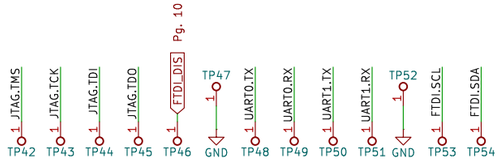






ICT Testpoints

Note:
Place on the bottom side



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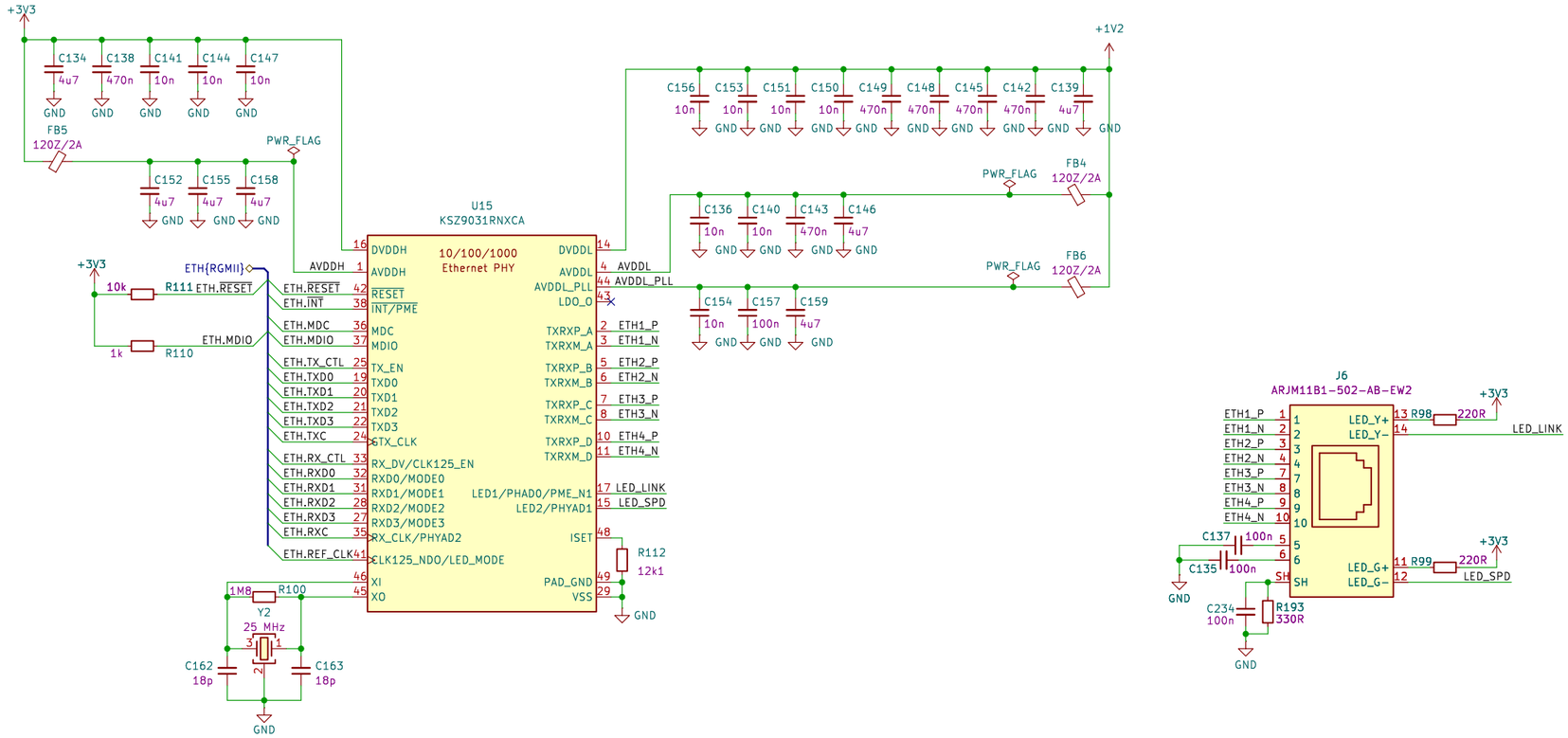
Sheet: /Debug FTDI/
File: debug-ftdi.kicad_sch

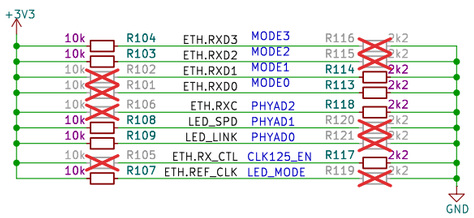
Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 6/17

Gigabit Ethernet

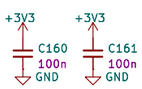


Bootstrap configuration



MODE[3:0] : 1100 (RGMII mode – Advertise 1000BASE-T full-duplex only)
PHYAD[4:0]: 00011
CLK125_EN: 0, disabled
LED_MODE: 1, Single-LED mode

Reference plane decoupling



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Sheet: /Ethernet/
File: ethernet.kicad_sch

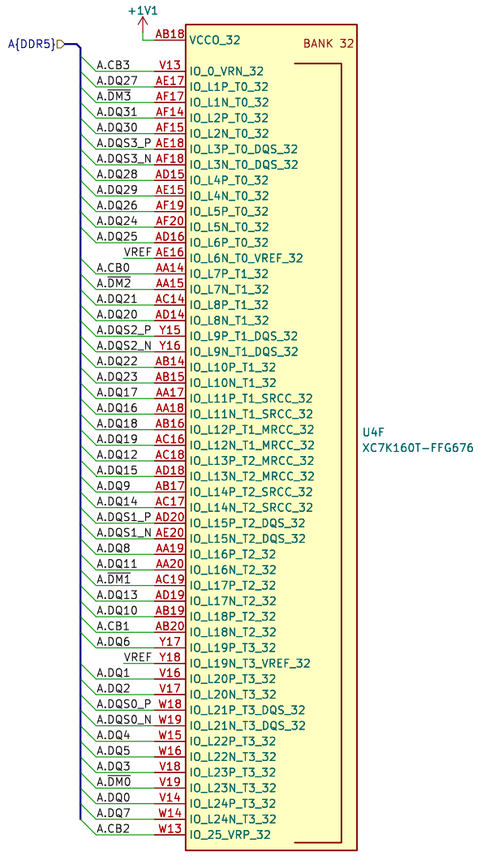
Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 8/17

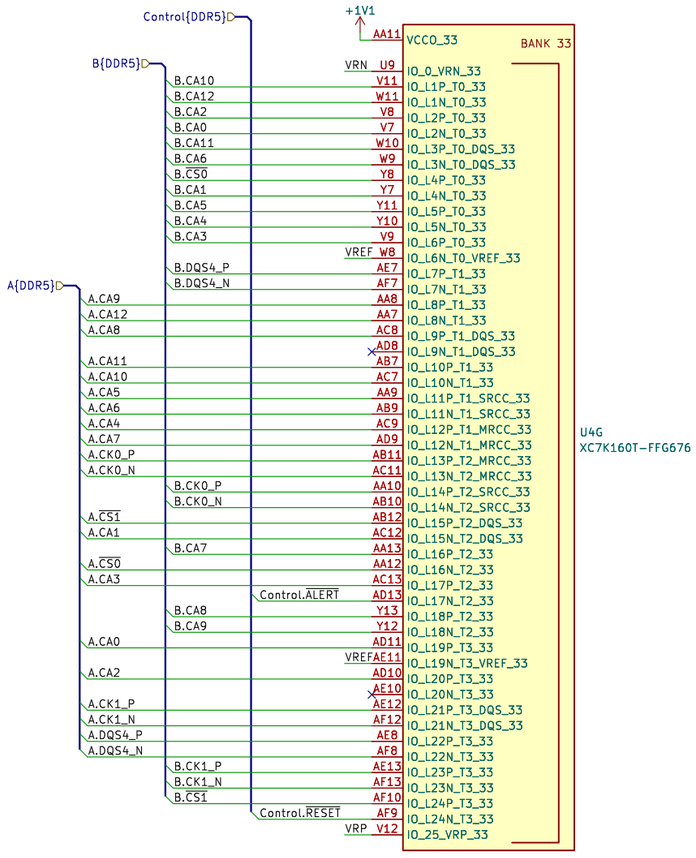
HP Banks

VCCO (HP banks) max: 2.0V

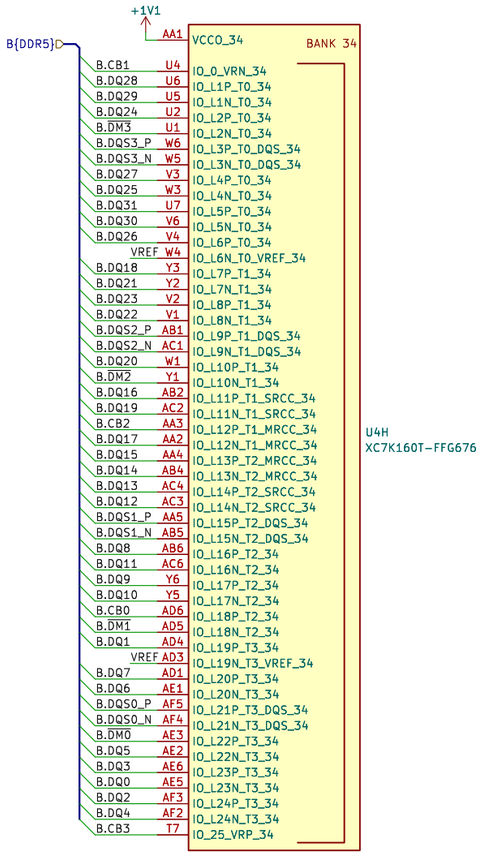
BANK 32



BANK 33

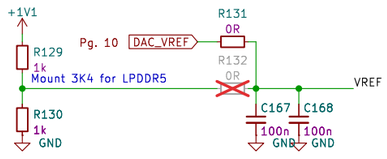


BANK 34

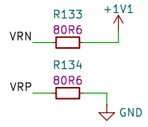


Pinout D.1.1

VREF



Reference termination



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Sheet: /FPGA banks HP/
File: fpga-banks-32-34.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265e7**
KiCad E.D.A. 9.0.6		Id: 9/17

Power source

J7 PJ-002AH
7–15V DC_PWR_AUX
F1 0466004.NR
12V_aux
12V_aux_fused
C169 100n
D16
PWR_FLAG
U17 LTC4412IS6
C175 100n
C179 1u/25V
ESDA25P35-1U1M
Q12 SI7613DN-T1-GE3
TP16
GND
PCIe_PWR
+12V
F2 0466004.NR
12V_PCIE_fused
C170 100n
U18 LTC4412IS6
C176 100n
C180 1u/25V
Q13 SI7613DN-T1-GE3
VDC

Always-ON +3V3 LDO

U21 NCP718BSN330T1G
VDC
+3V3_AON
PWR_FLAG
C181 1u/25V
C194 1u
TP19

ON/OFF Button controller

+3V3_AON
C195 100n
PB_CTRL_OUT
R149 47k
R160 47k
U22 MAX16150A_SOT
PB_CTRL_CLR
PB_CTRL_IN
PB_CTRL_INT
FPGA_POWER_OFF Pg. 15
Q14 BSS138PW,115
R161 47k
SW5 KMR211NGLFS

Power cycle

FPGA_POWER_CYCLE Pg. 15
R172 47k
R171 47k
Q16 BSS138PW,115
C203 100n
U26 MAX812REUS+T
SEQ_EN
Q17 BSS138PW,115
140ms delay fixed

Power supply sequencer

C212 100n
U31 LM3880
R184 47k
R187 47k
R190 47k
C209 100n
EN1
EN2
EN3

DC–DC INT

C200 22u_25V
C202 22u_25V
C204 100n
C208 100n
U27 MP8869S
1V0_BS
1V0_SW
L1 1u5/17A
R188 0R 22.4A
R189 0R 22.4A
1V0_REG
1V0_VCC
C201 470n
C213 22u
C215 22u
C217 22u
C219 22u
R181 10k
R185 80k6
C221 22p
R186 205k
C210 22n
1V0_FB
1V0_SS
PWR.SDA
PWR.SCL
EN1
PG1
I2C: 0x61

Config switch

+3V3_AON
R139 47k
R140 47k
SW4 SW_CVS-08TB
PB_CTRL_OUT1
PB_CTRL_INT2
SEQ_EN
PB_CTRL_CLR
PWR{I2C}
Pg. 17 IN1
Pg. 17 IN2
PWR_SDA_2
PWR_SCL_2
QDCDC2_SCL
Pg. 6 FTDI_DIS

NOTE:
1. AUTO ON/ PB-Controller
2. Bs off/ instant off
3. PWR I2C MUX input select 1
4. PWR I2C MUX input select 2
5. PWR I2C SDA disconnect from 3V3 powered IC's
6. PWR I2C SCL disconnect from 3V3 powered IC's
7. Connect QDCDC2 I2C
8. Disable FTDI JTAG

Power Monitors

U25 PAC1954T-E_VQFN
U30 PAC1954T-E_VQFN
R173 10k
R182 10k
I2C: 0x1F
I2C: 0x10
C199 100n
C214 100n
MGTAVCC_SEN_+
MGTAVCC_SEN_–
1V8_SEN_+
1V8_SEN_–
3V3_SEN_+
3V3_SEN_–
5V_SEN_+
5V_SEN_–
sp_SEN_+
sp_SEN_–
1V1_SEN_+
1V1_SEN_–
1V7_SEN_+
1V7_SEN_–
1V2_SEN_+
1V2_SEN_–

DC–DC AUX, MGT

U19 MPM54304GMN
C171 22u_25V
C177 22u_25V
C172 1u
C182 22u
C186 22u
C183 22u
C187 22u
C188 22u
C189 22u
R141 0R01
R142 0R01
R143 0R01
R144 0R01
+1V0_MGTAVCC
+1V8
spare
1V7
TP8
TP15
TP14
TP18
MGTAVCC_local
1V8_local
spare_local
1V7_local
Set to -1V7
R151 0R
R152 0R
R153 0R
R154 0R
R162 0R
R163 0R
R164 0R
R165 0R
NOTE: optional external divider
I2C: 0x68

Soft start delay time slot	1	2	3	4
MGTAVCC	X			
+1V8		X		
MGTAVTT		X		

DC–DC IO

U20 MPM54304GMN
C173 22u_25V
C178 22u_25V
C174 1u
C184 22u
C190 22u
C185 22u
C191 22u
C192 22u
C193 22u
R145 0R01
R146 0R01
R147 0R01
R148 0R01
+3V3
+5V
+1V1
+1V2
TP11
TP12
TP13
TP9
3V3_local
5V_local
1V1_local
1V2_local
R155 0R
R156 0R
R157 0R
R158 0R
R166 0R
R167 0R
R168 0R
R169 0R
FB5
FB6
FB7
FB8
QDCDC2_VCC
PWR.SDA
QDCDC2_SCL
PG3
I2C: 0x69

As both MPM54304GMN have same address (from factory), there is a need to cut SCL signals using dip switch

Soft start delay time slot	1	2	3	4
+3V3	X			
+5V				X
+1V1			X	
+1V2		X		

MGTAVTT Low noise LDO

U28 XC6230H001ER-G
C206 1u
R180 4k7
MGTAVTT_ILIM
MGTAVTT_OUT
R183 0R 22.4A
+1V2_MGTAVTT
1V2 Low noise
TP17
C211 10u

VREF DAC

U29 MCP4726A0T-E/MAY
C205 100n
C207 10u
C216 100n
C218 10u
C220 100n
DAC_VREF Pg. 9
I2C: 0x60

FAN connector

Q15 BSS138PW,115
R170 10k
C198 1u
J8 BM04B-SRSS-TB(LF)(SN)
Pg. 15 FAN_PWM
+5V

Power good

R135 47k
R136 0R PG1
R137 0R PG2
R138 0R PG3
Pg. 3 POWER

Ground probe pads

TP21 TP_1206_SMD_RCW-0C
TP20 TP_1206_SMD_RCW-0C

ICT Testpoints

TP25 VDC
TP26 +3V3_AON
TP27 +1V0
TP28 +1V0_MGTAVCC
TP30 +3V3
TP32 +1V2
TP34 +1V8
TP33 +1V1
TP35 +1V2_MGTAVTT
TP31 +5V
TP36 GND
TP55 PWR_SCL_21
TP56 PWR_SDA_21
TP29 1V7
Pg. 9 DAC_VREF
TP66
MGTAVTT_OUT
TP65
MGTAVCC_local
TP58
1V7_local
TP60
5V_local
TP61
1V1_local
TP62
1V2_local
TP63
3V3_local
TP64
1V0_REG
TP57
1V8_local
TP59
QDCDC2_SCL
TP71
Note: Place on the bottom side

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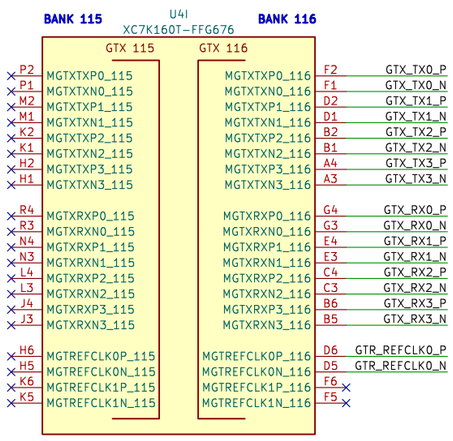
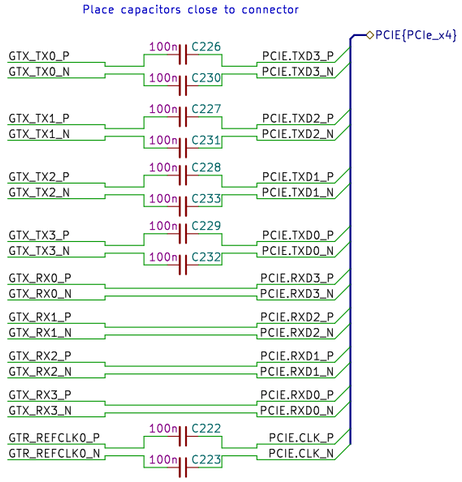
Sheet: /Supply/
File: supply.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3 | Date: 2025-11-26 | **Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6 | Id: 10/17

MGT Interface





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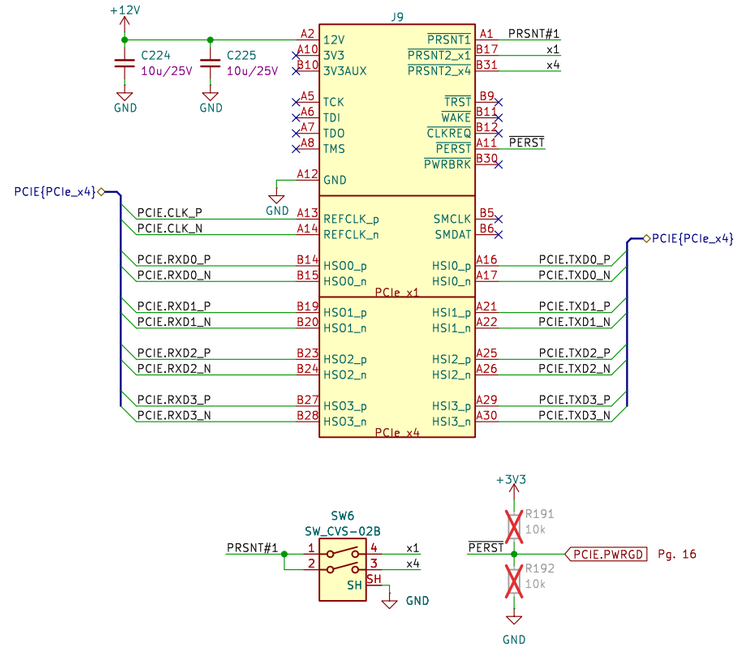
Sheet: /FPGA MGT Interface/
File: fpga-mgt.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 11/17

PCIe



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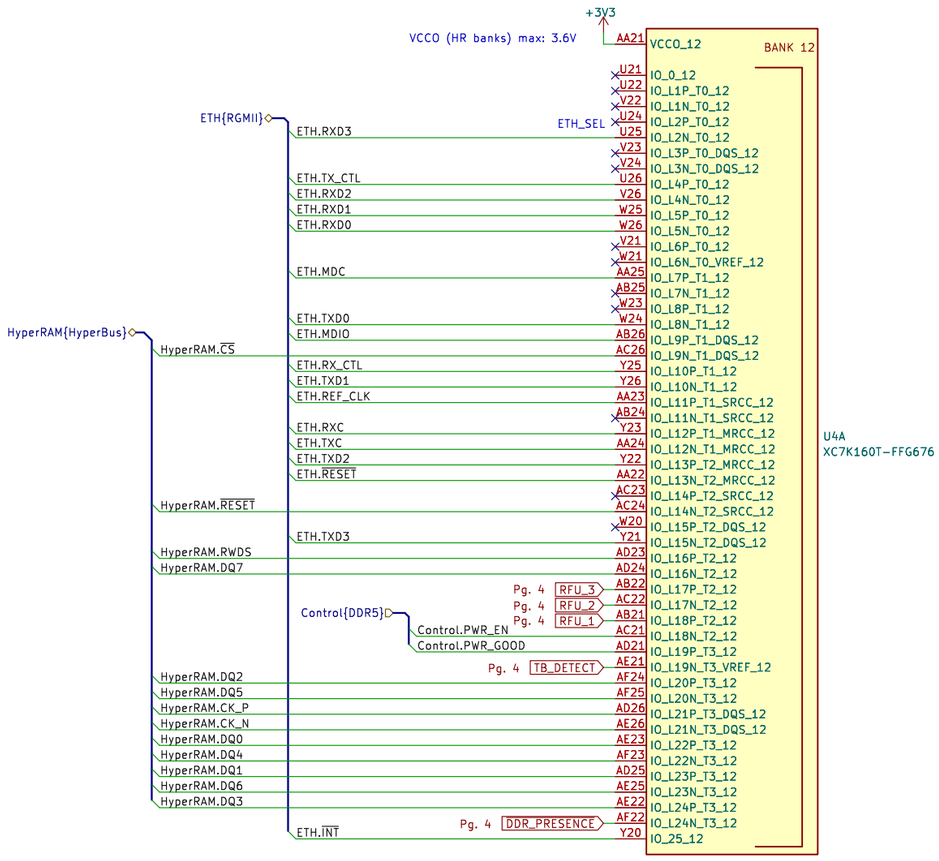
Sheet: /PCIe connector/
File: pcie-connector.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 12/17

BANK 12



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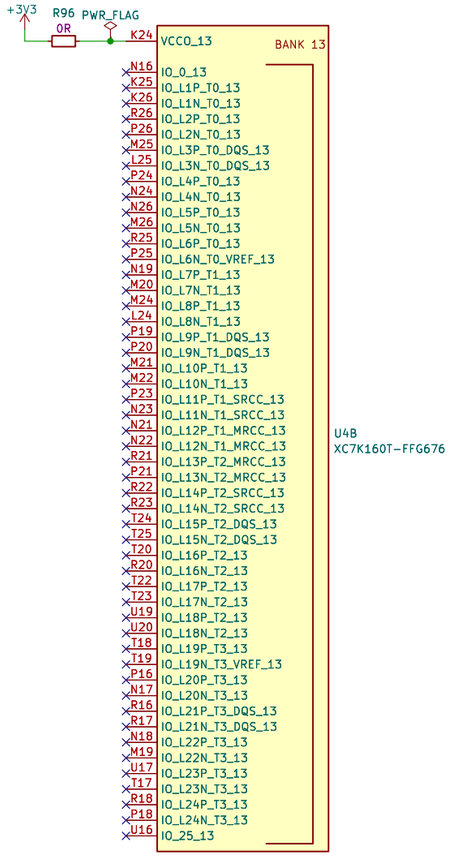
Sheet: /FPGA bank 12/
File: fpga-bank-12.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 13/17

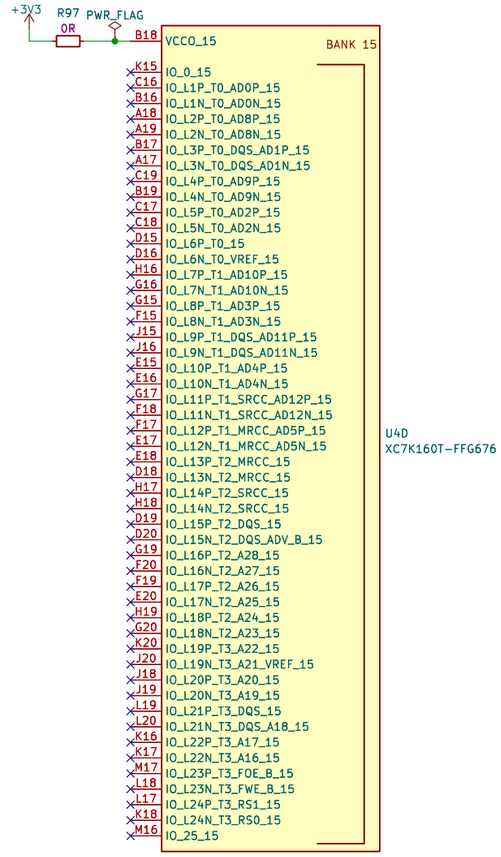
BANK 13

Connected to 3V3 for increased ESD protection



BANK 15

Connected to 3V3 for increased ESD protection



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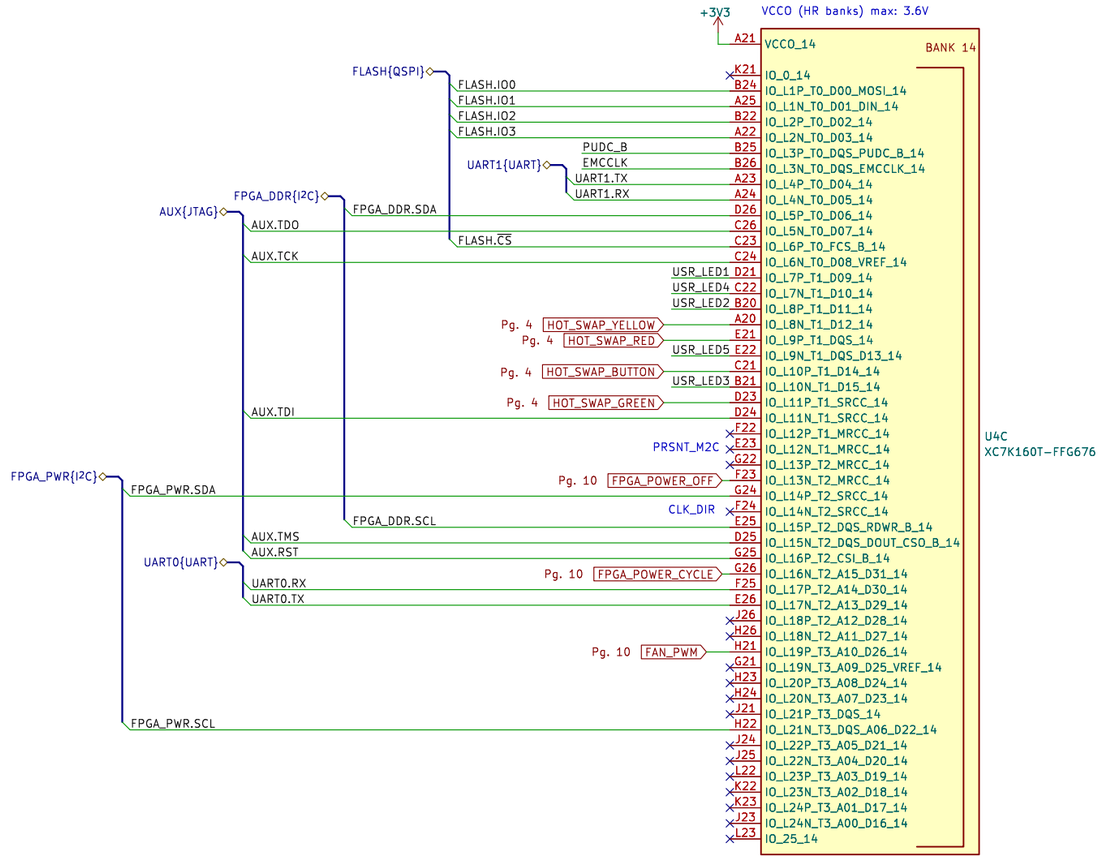
Sheet: /FPGA banks unused/
File: fpga-bank-13-15.kicad_sch

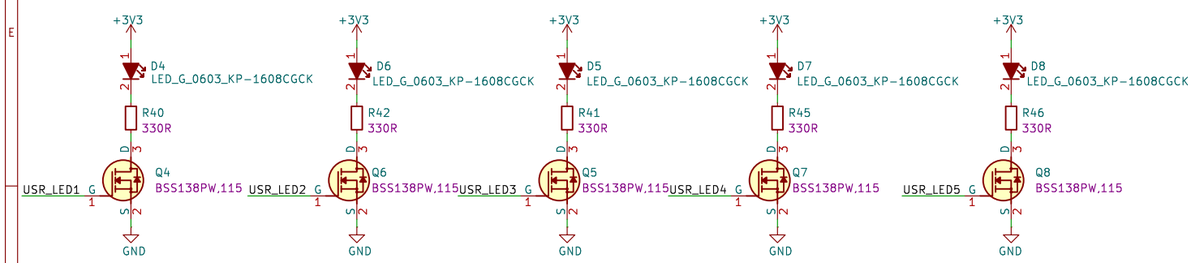
Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 14/17

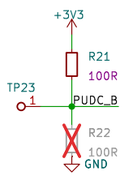
BANK 14



User LEDs



Probes



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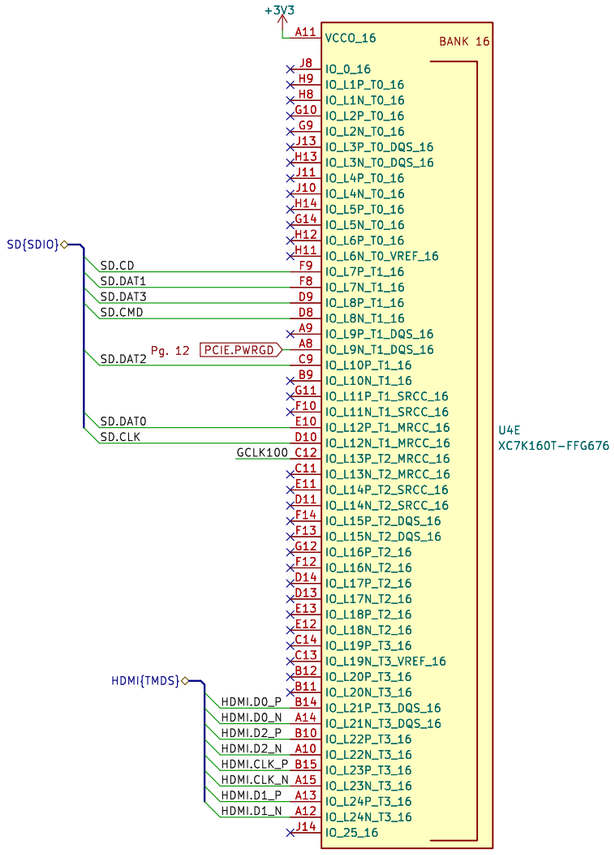
Sheet: /FPGA bank 14/
File: fpga-bank-14.kicad_sch

Title: SO-DIMM DDR5 Tester

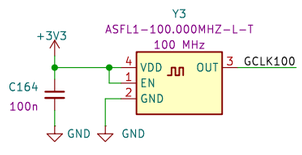
Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 15/17

BANK 16

VCCO (HR banks) max: 3.6V



Clock source



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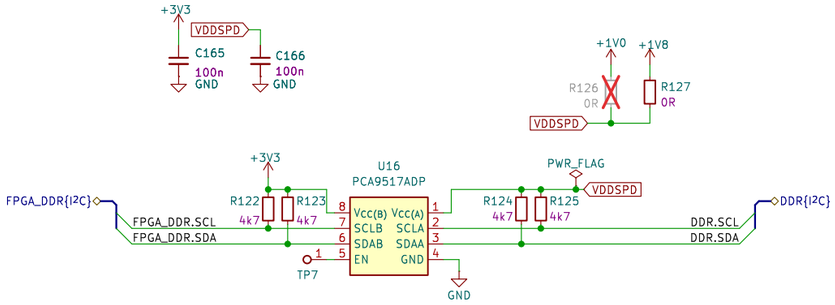
Sheet: /FPGA bank 16/
File: fpga-bank-16.kicad_sch

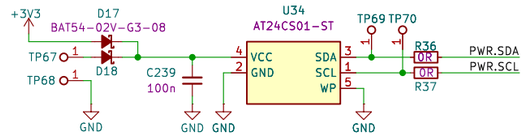
Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 16/17

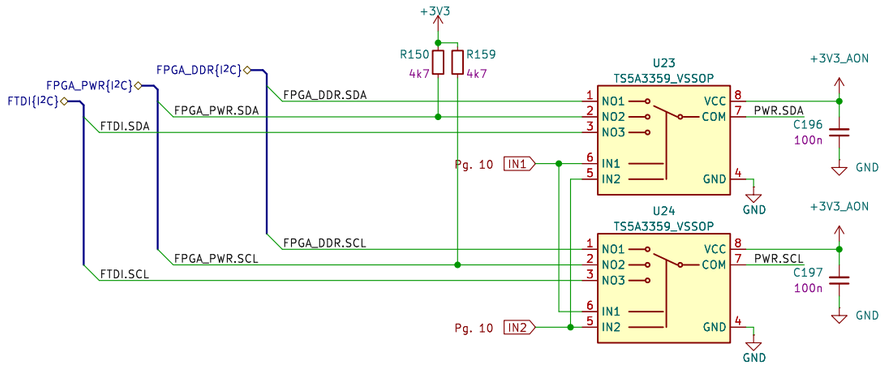
I2C logic translator



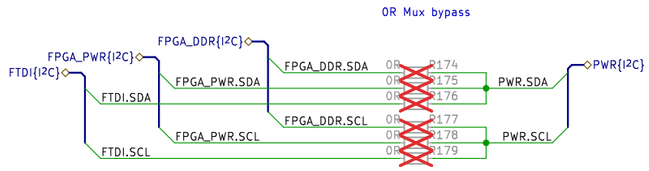
I2C EEPROM with unique ID



PWR I2C MUX

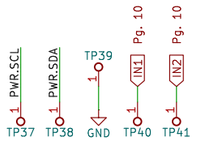


PWR I2C	IN1	IN2
OFF	L	L
FPGA DDR I2C	H	L
FPGA PWR I2C	L	H
FTDI	H	H



ICT Testpoints

Note:
Place on the bottom side



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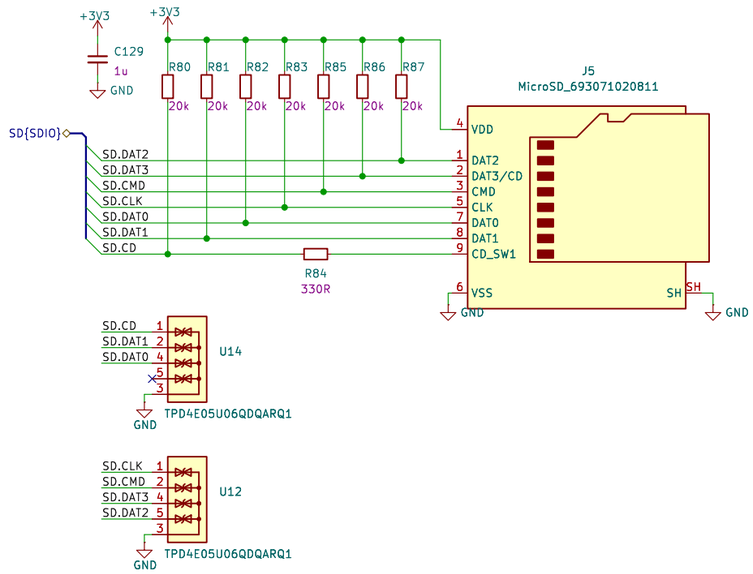
Sheet: /I2C/
File: i2c.kicad_sch

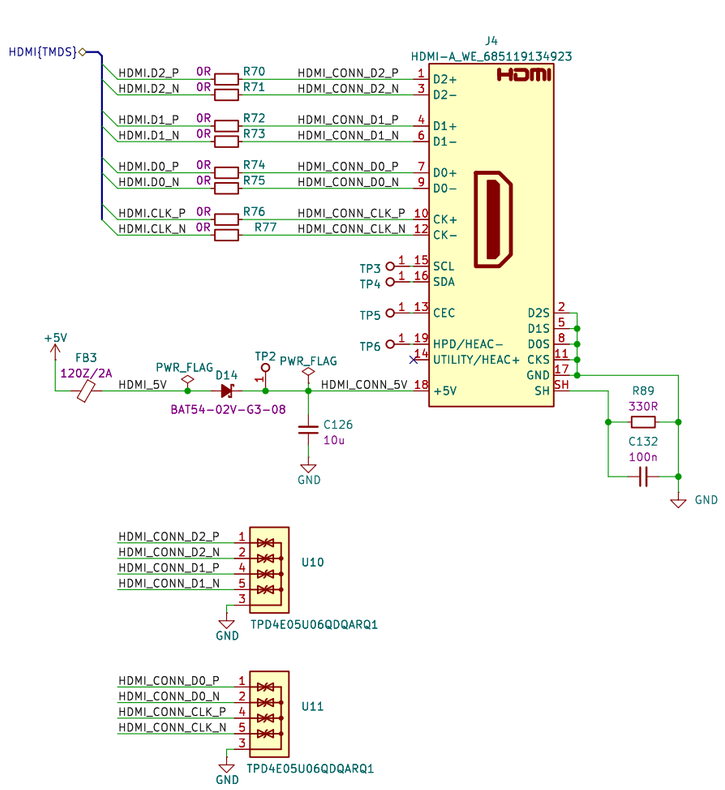
Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 17/17

SD card



HDMI



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Sheet: /HDMI + SD Card/
File: hdmi-sd-card.kicad_sch

Title: SO-DIMM DDR5 Tester

Size: A3	Date: 2025-11-26	**Rev: 1.3.0:05b265a7**
KiCad E.D.A. 9.0.6		Id: 17/17